On-Chip Combined C-V/I-V Characterization System in 45-nm CMOS Technology

Simeon Realov, *Member, IEEE*, and Kenneth L. Shepard, *Fellow, IEEE*

***Abstract*—An on-chip system for combined capacitance-voltage (C-V) and current-voltage (I-V) characterization of a large integrated transistor array implemented in a 45-nm bulk CMOS process is presented. On-chip I-V characterization is implemented using a four-point Kelvin measurement technique with 12-bit sub-10 nA current measurement resolution, 10-bit sub-1 mV voltage measurement resolution, and sampling speeds on the order of 100 kHz. C-V characterization is performed using a novel leakage- and parasitics-insensitive charge-based capacitance measurement (CBCM) technique with atto-Farad resolution. The on-chip system is employed in studying both random and systematic sources of quasi-static device variability. For the first time, combined C-V/I-V characterization of circuit-representative devices is demonstrated and used to extract variations in the underlying physical characteristics of the device, including line-edge-roughness (LER) parameters and systematic device length variations across the die.**

***Index Terms*—Atto-Farad, CBCM, characterization, CMOS, on-chip, C-V, I-V, LER, variability, 45 nm.**

I. Introduction

THE steady increase in transistor variability with each new technology node demands novel approaches to device characterization that enable the detailed study of large transistor statistical sample sets with high measurement throughput. On-chip integration of dense addressable test arrays is an attractive approach for acquiring such data. Traditionally, most work has focused on ring-oscillator-based [1], [2], or, more generally, delay-based test structures [3], [4], which offer high measurement throughput and performance-centric characterization. However, such structures ultimately rely on circuit delay as a singular metric of device performance. While this metric is indeed comprehensive, it fails to give specific information regarding the underlying physical sources of device variability; such information is critical for accurate statistical modeling as well variability mitigation through modification of the manufacturing process.

Other on-chip techniques focus on current-voltage (I-V) characterization of integrated transistor [5], [6] or SRAM [7] test arrays using sophisticated off-chip analog characterization equipment. While more detailed characterization can be performed in this manner, off-chip measurements significantly impact the throughput of such systems and make the gathering of large amounts of statistical data cumbersome. Additionally, a pure I-V characterization methodology completely ignores variability in the capacitance-voltage (C-V) characteristics of the device, and as such, gives only a partial representation of the impact of device variability on circuit performance.

In order to overcome some of the problems associated with off-chip characterization, efforts have been made to integrate analog characterization circuitry on the same die as the device-under-test (DUT) array [8], [9], where integrated analog-to-digital (ADC) converters are used to perform digitally-interfaced analog on-chip I-V characterization. Such high levels of test integration have the potential to yield high measurement throughput but do not address limitations associated with the lack of C-V characterization.

In this work, an on-chip system for characterization of large addressable transistor DUT arrays is presented [10]. The system offers fully-integrated C-V/I-V measurement capability for circuit-representative NMOS and PMOS devices with high measurement throughput and a purely digital interface. Section II describes the design of the on-chip characterization system and its individual components. Section III describes different techniques developed to enable rapid and comprehensive C-V/I-V on-chip characterization, including a novel leakage-insensitive charge-based capacitance measurement (CBCM) technique with atto-Farad resolution. Section IV discusses measurement results related to characterization of the on-chip measurement system as implemented in a 45-nm CMOS process, as well as results of combined C-V/I-V variability measurements on circuit-representative devices in this process. The benefits of the combined C-V/I-V characterization approach are demonstrated through extraction and analysis of small-signal transconductance and intrinsic gate capacitance variability data, where both random and systematic variability is observed. The underlying dominant physical sources of device variability reflected in these two parameters are decoupled through cross-correlation between the C-V and I-V measurement results. Section V concludes.

II. System Design

Fig. 1 shows a simplified top-level schematic of the on-chip characterization system. The system consists of three major blocks—an on-chip switching matrix, used to individually address transistors from the device-under-test (DUT) array; a four-channel digital-to-analog converter (DAC), used to supply each of the four DUT terminal bias voltages; and a

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S. Realov and K. L. Shepard are with the Department of Electrical Engineering, Columbia University, New York, NY 10027 USA (e-mail: srealov@ee.columbia.edu).

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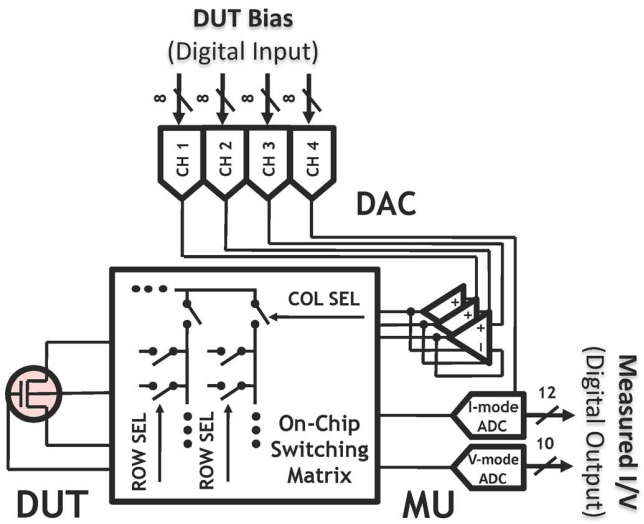


Fig. 1. A simplified top-level schematic of the on-chip characterization system.

measurement unit (MU), which consists of a current- and voltage-mode analog-to-digital converters (ADCs), used to perform accurate on-chip I-V and charged-based C-V characterization. The system has a digital-in/digital-out measurement interface, making it compatible with a purely digital test flow. The only externally-supplied analog signals are dc current and voltage references as required by the DAC and ADCs. All analog circuitry is designed using high-voltage thick-oxide I/O devices. While inherently much slower than thin-oxide devices, these devices offer significantly higher intrinsic gain and increased voltage headroom, greatly simplifying the robust implementation of accurate analog functionality. The system can be configured to characterize both NMOS as well as PMOS devices by adjusting the analog references and internal controls to account for opposite current polarities.

A. On-Chip Switching Matrix and DUT Array

A simplified representation of the DUT array and the accompanying switching matrix is shown in Fig. 2(a); a detailed representation of a single NMOS DUT array cell and all accompanying switches is shown in 2(b). Column-select and row-select signals from one-hot shift registers are used to sequentially access individual DUTs from the array. Switches in the array are implemented using thick-oxide CMOS transmission gates, offering higher on-to-off current ratios and operating at a higher maximum voltage as compared to native-oxide devices. The DUT array spans 40 rows of DUTs across 56 columns. Each column contains 39 identical DUTs, in addition to one empty array cell used as a null reference. Two neighboring columns contain matched DUTs of the same type, as indicated in Fig. 2(a), allowing any gradients across the length of the DUT column to be cancelled out differentially. Overall, the measurement sample set consists of 28 different DUT types with devices spanning different lengths, widths, threshold voltages, and environments, with a statistical set size of 78 DUTs per DUT type. Two test arrays containing NMOS and PMOS DUTs are interleaved, sharing many of the common global digital control signals, but with completely

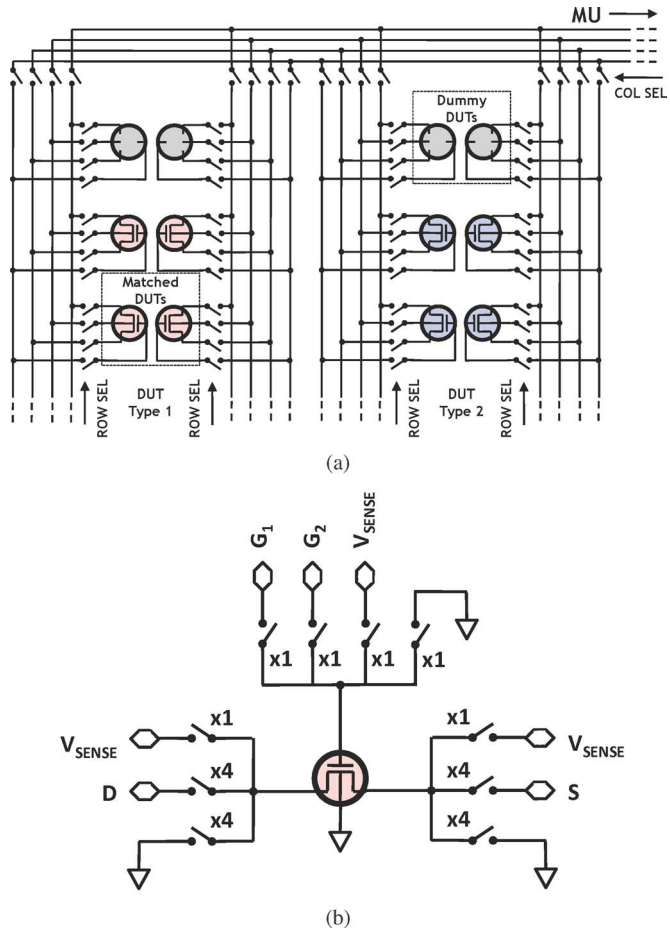


Fig. 2. (a) A simplified schematic of the DUT array and associated on-chip switching matrix and (b) a detailed schematic of an NMOS DUT and all associated sampling switches with relative sizing indicated as multiples of a minimum-size switch.

electrically isolated analog signal paths and dedicated on-chip characterization circuits.

B. DAC

A four-channel resistor-string DAC is used to provide each of four DUT terminal voltages (Fig. 3.). The four DAC channels share the same resistor string reference, and each channel has 256 different output levels, resulting in eight-bit resolution. The control of the DAC output is implemented using four independent one-hot bi-directional shift registers, ideally suited for generating voltage sweeps. Each of the channels is buffered using a single-stage load-stabilized analog voltage buffer. These simple buffers are designed to drive purely capacitive loads as the analog DAC outputs are routed from the DAC to the MU, where more sophisticated high-gain, low-output-impedance unity-gain buffers are used to bias the DUTs.

C. Measurement Unit (MU)

The measurement unit (MU) consists of both current- and voltage-mode ADCs, as needed to perform accurate I-V and charged-based C-V device characterization. The two ADCs are based on a dual-slope integrator topology, which offers excellent measurement characteristics, including high tolerance to variation in the passive components [11] and high immunity to noise and other interference [12]. Both ADCs are implemented

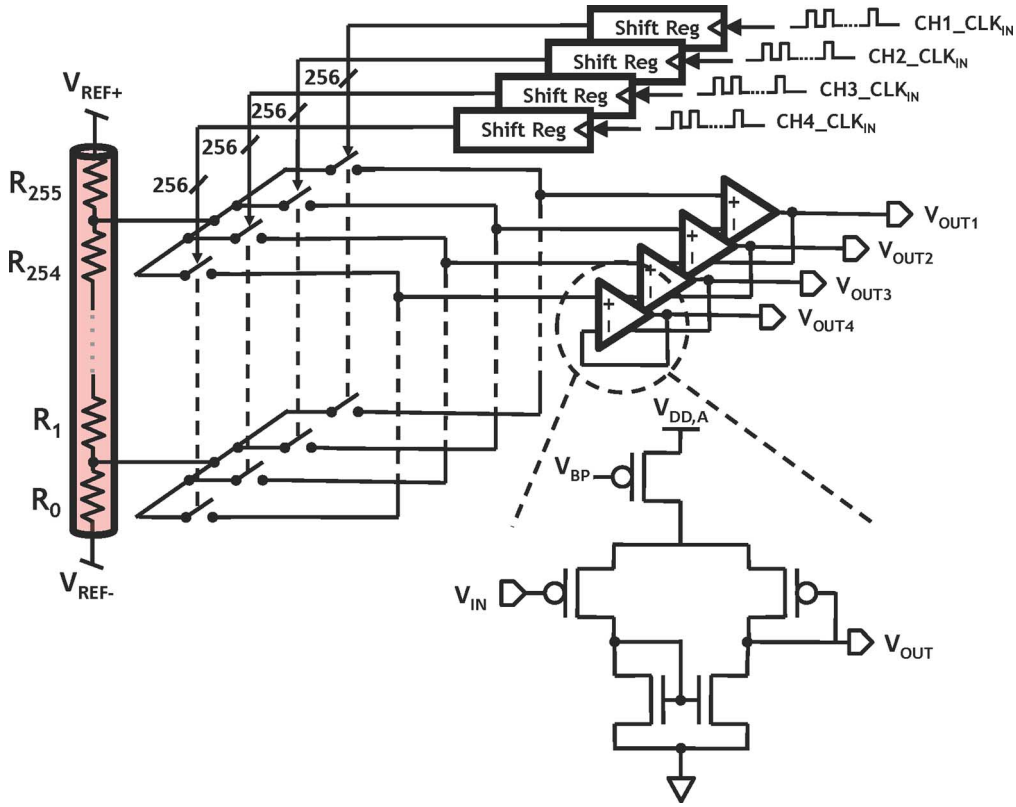


Fig. 3. Four-channel R-string DAC with one-hot shift register control used for generating DUT bias voltages.

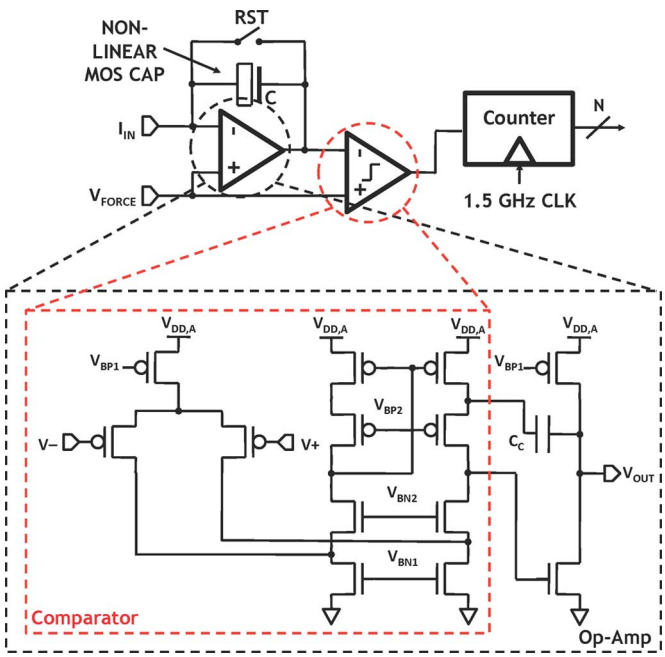


Fig. 4. Dual-slope integrator core and associated op-amp and comparator circuit implementation.

around the same integrator core, making the overall system design modular.

1) Integrator Core: The integrator core, shown in Fig. 4, consists of a two-stage op-amp, a non-linear MOS capacitor, a high-gain comparator, and a high-speed digital counter. The input stage of the op-amp is implemented as a folded-cascode and has a simulated gain of 90 dB; the output stage has a common-source topology and a simulated output impedance of less than 500 Ω. High gain is needed to achieve high conversion accuracy while low output impedance is essential for driving low-impedance loads, such as wide DUTs biased in strong inversion. An 80-pF non-linear thick-oxide MOS capacitor is used as the main integrating element; it offers higher charge density as compared to other capacitor options and is readily available even in purely digital design flows. Since dual-slope integration is based solely on the concept of charge conservation, the non-linearity of the capacitor does not affect the linearity of the ADCs, as long as it does not leak or absorb charge during the conversion cycle. The comparator is implemented using a copy of the folded-cascode op-amp input stage of Fig. 4. A high-speed counter used to time the charge and discharge cycles of the integrator is implemented using native 45-nm devices, which allows it to operate at frequencies of 1.5 GHz and above. Leveraging the intrinsic speed of the underlying 45-nm CMOS process is essential to achieving high performance from the integrator core as a high clock rate enables higher converter precision for a given sampling rate, or equivalently, an improved sampling rate for a given measurement precision.

2) Current-Mode ADC: The integrator core is easily converted into a current-mode ADC, as shown in Fig. 5(a). The potential, V_F, supplied by one of the DAC channels, is forced at the input of the ADC though the negative feedback of the integrator, setting the voltage bias of current input node. The output of the current-mode converter is given by

$$I_{\mathrm{IN}} = N_{\mathrm{OUT}} \frac{I_{\mathrm{REF}}}{N_{\mathrm{REF}}} \tag{1}$$

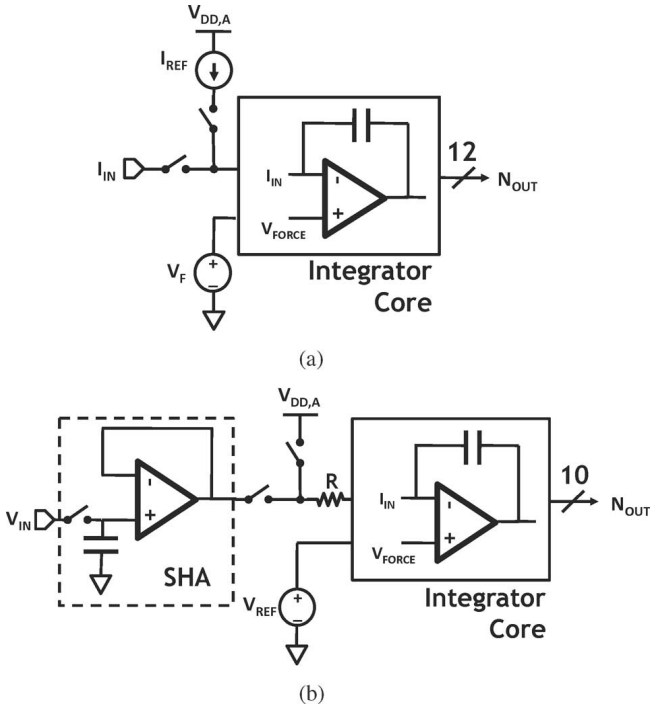


Fig. 5. (a) Current-mode ADC configuration and (b) voltage-mode ADC configuration using dual-slope integrator core. (a) I-mode, (b) V-mode.

where $I_{\rm REF}$ is the reference current, $N_{\rm REF}$ is the integration time expressed in number of reference clock cycles, and $N_{\rm OUT}$ is the measured digital output. From (1), the nominal $I_{\rm LSB}$ of the converter is given by $(I_{\rm REF})/(N_{\rm REF})$. The $I_{\rm LSB}$, and consequently, the dynamic range of the converter can be adjusted by either increasing the integration time or decreasing the reference current.

3) Voltage-Mode ADC: The implementation of the voltage-mode ADC is shown in Fig. 5(b). A simple sample-and-hold amplifier (SHA) is used to sample and buffer the input voltage. The SHA guarantees high input impedance, which is essential for proper four-point Kelvin measurements, and is based on the op-amp of Fig. 4 in a unity-gain-feedback configuration. A large 10-pF sampling capacitor diminishes errors due to charge injection from the sampling switch, and a 25-kΩ resistor converts the sampled voltage to a dc current to be processed by the integrator core. The output of the converter is given by

$$V_{\rm OUT} = V_{\rm REF} - N_{\rm OUT}\frac{V_{{\rm DD},A} - V_{\rm REF}}{N_{\rm REF}} \tag{2}$$

where $V_{\rm REF}$ is the reference voltage (defined with respect to a ground potential), $V_{{\rm DD},A}$ is the analog supply voltage, $N_{\rm REF}$ is the integration time expressed in number of reference clock cycles, and $N_{\rm OUT}$ is the measured digital output; $V_{\rm LSB}$ is set by $(V_{{\rm DD},A} - V_{\rm REF})/(N_{\rm REF})$. While the value of the resistor, R, does not factor into the conversion equation, the linearity of the converter is directly related to the linearity of the resistor, unlike the case with the integration capacitor. Therefore, in order to achieve high linearity, a poly-silicon resistor option is used to implement resistor R.

4) Biasing Buffers: Unity-gain analog buffers are used to bias the DUT terminals not connected to the current-mode ADC.

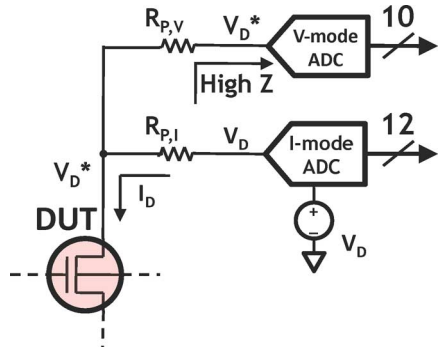


Fig. 6. Four-point Kelvin measurements to negate parasitic IR drops through the on-chip switching matrix.

The DAC buffers shown in Fig. 3 are not suitable for driving real loads with high accuracy, and are only used as high-input-impedance buffers between the internal resistor-string outputs and the unity-gain buffers in the MU. The MU buffers, which drive low-impedance paths going to the source/drain terminals of the DUT, are implemented using copies of the two-stage op-amp of Fig. 4. High-impedance paths biasing the gate and the body of the DUT, on the other hand, are driven by unity-gain buffers implemented using a scaled-down version of the folded-cascode input stage of the same op-amp.

III. Measurement Techniques

We have developed I-V and C-V measurement techniques which exploit the circuitry of Section II. Issues related to non-negligible parasitic resistances through the on-chip switching matrix need to be addressed when performing I-V characterization. In addition, we have implemented a charge-based capacitance measurement (CBCM) methodology for quasi-static C-V characterization which allows capacitance measurements to be performed with the same measurement infrastructure. This CBCM technique addresses issues related to gate leakage through the DUT, parasitic leakages and capacitances from the on-chip switching matrix, and measurement noise to achieve the desired atto-Farad resolution levels.

A. I-V Measurements

A four-point Kelvin measurement approach (Fig. 6) is used for accurate I-V characterization in the presence of non-negligible parasitic resistance through the on-chip switching matrix due to both the wiring parasitics and the resistance of the access switches. While the virtual ground supplied by the integrator at the input of the current-mode ADC accurately sets a bias for the current measurement to be performed, an IR drop across the parasitic resistance in the current path, $R_{P,I}$, causes the applied voltage V_D^* at the terminal of the DUT to decrease as a function of the measured current,

$$V_D^* = V_D - I_D R_{P,I}, \tag{3}$$

where I_D is the current through the DUT, and V_D is the desired DUT terminal voltage bias. To eliminate the effect of these parasitic resistances, V_D^* is directly measured using a secondary sense path. The parasitic resistance in the sense path, $R_{P,V}$, does not affect the measured voltage due to the high input impedance

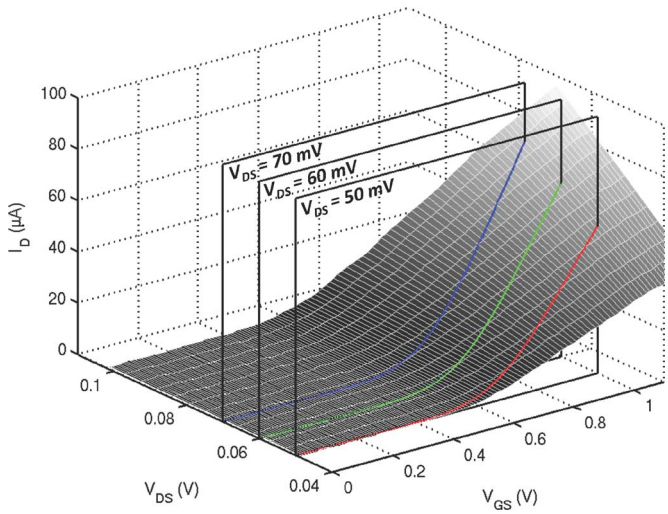


Fig. 7. Measured I_D surface as a function of V_{GS} and V_{DS}; I_D values can be interpolated along planes of constant V_{DS} potential as shown.

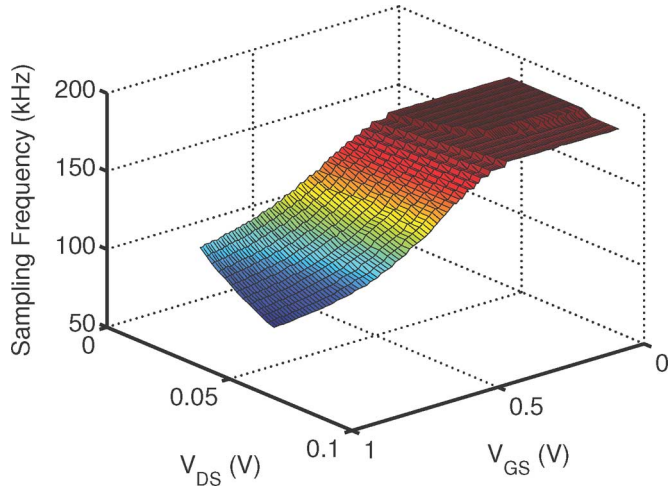


Fig. 8. Signal-strength-optimized sampling frequency across a 16 × 256 point linear I-V sweep of a $W/L = 1.0\ \mu$m/0.04 μm device; the sampling frequency varies between 185.2 kHz and 84 kHz resulting in more than 80% improvement in overall characterization time.

of the voltage-mode ADC. Since the current at a DUT terminal is potentially a function of all four terminal bias voltages, the voltage at each of the DUT terminals is measured through individually designated voltage sense paths. Sampling all four DUT terminals removes any measurement uncertainty due to offsets in the biasing unity-gain buffers.

Even though the DUT array allows voltage and current sense paths to be routed to any one of the four DUT terminals (with the exception of the body of NMOS DUTs, which is tied to the substrate potential of the chip), characterizing the drain current, I_D, as a function of the gate-to-source bias, V_{GS}, for a constant drain-to-source bias, V_{DS}, is the primary focus of this work. By sweeping the applied gate and drain voltages, a three-dimensional surface plot of I_D as a function of V_{GS} and V_{DS} can be measured, as shown in Fig. 7. Since the voltage sweep steps given by the V_{LSB} of the DAC are as small as 4.3 mV, linear interpolation can be used to accurately extract the measured drain current across planes of constant V_{DS} bias. Although I_D is derived for a constant V_{DS}, V_{SB} does vary slightly over the bias range due to the series resistance introduced by the access switch at the source terminal of the DUT. If desired, this slight bias dependence can also be removed by sweeping the bias voltage applied at the source.

While typically analog-to-digital converters sample signals at a given characteristic sampling frequency, the dual-slope integrator ADCs can be configured to vary the sampling frequency according to the strength of the measured signal. The period needed to complete a conversion cycle is a function of the pre-charge time, which is set by the desired dynamic range, and the discharge time, which is determined by the signal strength. When operated in a synchronous fashion, the ADC sampling frequency needs to be configured to accommodate the maximum discharge time corresponding to the maximum allowable input current. However, when the I-V measurements considered are dc measurements, maintaining a constant sampling frequency is not required. Instead, the sampling time can be adjusted according to signal strength, yielding significant characterization time savings. Such optimal signal sampling is achieved by asynchronously triggering the beginning of a new conversion cycle on the comparator output signaling the completion of the previous sampling cycle. In a typical measurement, such as the one shown in Fig. 8, over 80% improvement in overall characterization time can be realized.

B. C-V Measurements

Traditionally, device capacitance-voltage (C-V) characterization is performed on large DUTs with direct access to the DUT terminals through pads on the die [13]. This approach is not only limited in the number of DUTs that can be integrated on the same chip, but it also fails to characterize variability at circuit-representative device geometries or to extract any correlation between the C-V and I-V characteristics. Additionally, as the oxide thickness scales, gate leakage due to quantum tunneling shunts the gate capacitance, making accurate C-V characterization challenging [14]. In order to address all of these issues, a quasi-static approach to C-V characterization is developed.

The CBCM technique developed here addresses these issues, achieving atto-Farad resolution. CBCM techniques have been used previouly in back-end-of-line (BEOL) characterization to extract the coupling capacitance between wires in the metal stack [15], [16]. More recently, these techniques have also been used for device characterization [13], [17], [18].

1) CBCM Measurement Technique: The leakage- and parasitic-insensitive on-chip CBCM technique is illustrated in Fig. 9 for the case of characterizing the gate-to-channel MOS capacitance, C_{GC}. During the first phase of the measurement, the DUT is biased at the desired operating point, with its gate connected to a potential V_G, and the drain and source connected to a potential V_C. Once this bias point has been established and all of the DUT potentials are stabilized, the current-steering switch at the gate flips, making the on-chip current-mode ADC the new source for the gate bias, which remains at V_G. At this point, the current necessary to maintain the bias at the gate starts being measured. After a short on-chip-generated delay on the order of

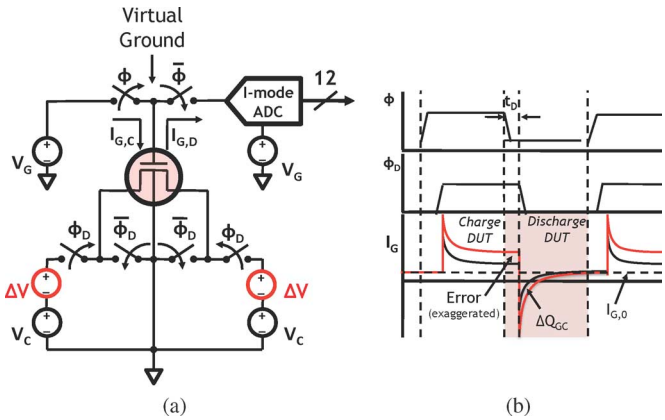


Fig. 9. Illustration of the leakage-insensitive CBCM technique applied to measuring C_{GC} of an NMOS transistor (a), and the accompanying waveforms (b); the shaded portion of the I_C plot indicates the measured discharge current $I_{G,D}$.

100 ps (denoted as t_D in Fig. 9(b)), the drain and source of the DUT are shorted to ground, causing C_{GC} to be discharged. The change of charge needed to keep the potential of the gate at V_G is integrated by the current-mode ADC, along with any leakage current through the device and the associated switching matrix (not shown). Once this charge transfer has settled, the DUT gate is disconnected from the measurement circuitry, and the DUT channel is once again biased at V_C. This cycle is repeated multiple times, building up a measurable amount of charge in the current-mode ADC.

At the end of the conversion, the measured charge, $Q_{G,M}(V_{GC})$, which is derived from the average discharge gate current, $I_{G,D}(V_{GC})$, can be expressed as

$$Q_{G,M}(V_{GC}) = \int_{T/2}^{T} I_{G,D}(t)\,\mathrm{d}t = Q_G(V_{GC}) + Q_{G,0}(V_G). \quad (4)$$

$Q_{G,M}(V_{GC})$ consists of $Q_G(V_{GC})$, which represents the gate charge due to the discharging of C_{GC}, and the charge $Q_{G,0}(V_G)$, which represents the charge due to an integrated error current. The error current, denoted as $I_{G,0}$ in Fig. 9(b), includes leakage currents through the DUT and the switching matrix, charge injection currents from the switch at the input of the ADC, leakage currents due to mismatches between the two nominally identical gate potentials, and any charge sharing currents from the parasitic capacitance at the gate node due to the same mismatch. $I_{G,0}$ is a function of the gate voltage, V_G, and is largely independent of the channel potential, V_C, and, consequently, the gate-to-channel potential, V_{GC}. This results from the fact that the error current is accumulated during the discharge phase of the cycle, where the bias conditions on the DUT are always constant—V_G at the gate and ground at all other terminals. This is in contrast to the gate charge, $Q_G(V_{GC})$, which is a function of the bias voltage applied during the charging step of the cycle and, therefore, varies with V_{GC}.

The gate-to-channel capacitance, C_{GC}, is given by

$$C_{GC}(V_{GC}) = -\frac{\partial Q_G(V_{GC})}{\partial V_{GC}}. \quad (5)$$

Even though it is difficult to decouple $Q_G(V_{GC})$ from $Q_{G,0}(V_G)$, we note that $Q_{G,0}(V_G)$ is a function of V_G only (and not V_{GC}), so as long as V_G is kept constant throughout the measurement, differentiating the measured charge, $Q_{G,M}(V_{GC})$ with respect to V_{GC} yields

$$-\frac{\partial Q_{G,M}(V_{GC})}{\partial V_{GC}} = -\frac{\partial Q_G(V_{GC})}{\partial V_{GC}} = C_{GC}(V_{GC}). \quad (6)$$

Therefore, by keeping V_G constant while V_C is swept, the combination of the effective virtual ground at the gate and the differential nature of CBCM can be leveraged to cancel out the errors due to $I_{G,0}$. The only error signal remaining is the leakage current integrated for the duration t_D (see Fig. 9(b)), which is in fact a function of V_C. However, since t_D is an on-chip generated delay of only about 100 ps, the negligibly small error accumulated in this time interval is the same as that in a standard CBCM measurement with a measurement frequency of 5 GHz.

Fig. 10 examines the effect of the CBCM measurement clock frequency, f_{CLK}, on measured $Q_{GC,M}$ as well as the extracted C_{GC}. Example measurements for the case of a PMOS and an NMOS transistors with $W/L = 1.0\ \mu$m/0.11 μm are considered. As expected, linearly decreasing the period of the measurement clock, T_{CLK} (or equivalently, increasing the measurement frequency, f_{CLK}), proportionally shifts the measured PMOS $Q_{GC,M}$ up and the measured NMOS $Q_{GC,M}$ down; the different directions of the shift are explained by the different polarities of the leakage current, $I_{G,0}$. More importantly, however, these shifts are constant across the measurement bias range, and result in no appreciable change in the extracted C_{GC}, as seen in Fig. 10(b); externally supplied CBCM clock frequency, f_{CLK}, as high as 20 MHz is supported by the measurement circuits, speeds not attainable with off-chip measurement techniques.

2) CBCM Data Post-Processing Techniques: In order to achieve atto-Farad (aF) resolution, a combination of oversampling and filtering techniques are used. If a voltage step $\Delta V = 4.3$ mV is considered, the average change of charge, ΔQ, which needs to be measured in order to resolve a capacitance of 1 aF is $4.3 \times 10^{-21}\ C$. This is less than one elementary charge, and at a measurement frequency of 20 MHz, results in an average current of 8.6 fA.

The nominal I_{LSB} of the current-mode ADC is decreased to $I_{\mathrm{LSB}} = 390.6$ pA by setting $N_{\mathrm{REF}} = 1024$ and $I_{\mathrm{REF}} = 400$ nA. Since the current measured to derive $Q_G(V_{GC})$ is a dc current, oversampling can be leveraged to further reduce the effective I_{LSB} of the converter. In particular, if an oversampling ratio (OSR) of 2^{11} is used, I_{LSB} is reduced to 190.7 fA, while an OSR of 2^{15} gives an I_{LSB} of 11.92 fA. Unfortunately, even with an aggressive CBCM clock frequency of 20 MHz, a full 256-point C-V measurement at an OSR of 2^{15} has an overall run time of approximately 12 min, which is prohibitively large for high-throughput studies.

To further suppress measurement noise, a Savitzky-Golay filter [19], particularly suited for extracting smooth derivatives from measured data, can be used. The Savitzky-Golay filter works by performing a polynomial fit through a moving data window, and using the fitted polynomial parameters to estimate the derivative of the data at the mid-point of the window. The

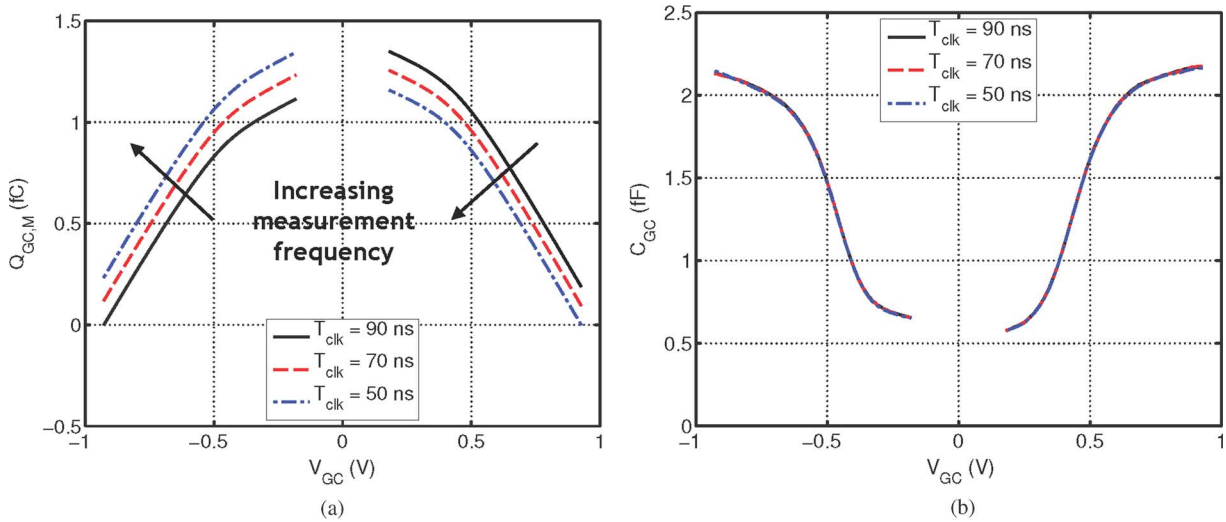


Fig. 10. Q_{GC} (a) and C_{GC} (b) measured at different CBCM clock frequencies for a PMOS (*left*) and an NMOS (*right*) device; while Q_{GC} changes with frequency, the extracted C_{GC} remains constant.

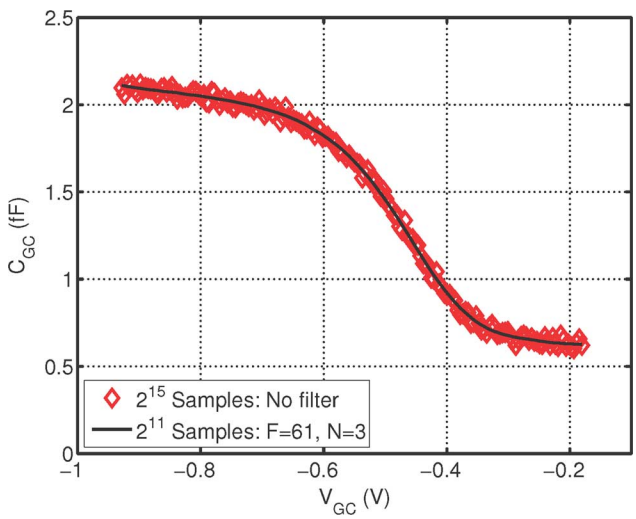


Fig. 11. Application of the Savitzky-Golay digital filter; the effectiveness of filtering in comparison to increasing the oversampling ratio is demonstrated.

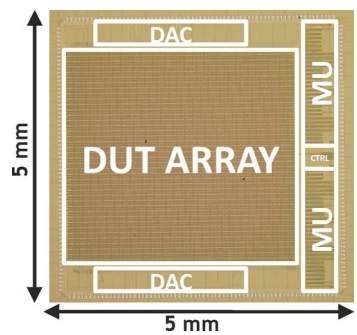


Fig. 12. A micrograph of the system implemented in a 45-nm CMOS process.

application of such a filter is tantamount to oversampling, where the knowledge that the data does not change rapidly within a given interval is used to better estimate a single-point value based on an ensemble of neighboring points. The size of the moving window, F, and the order of the fitted polynomial, N, are parameters of the filter, which must be chosen to achieve the desired noise reduction, while maintaining the high-frequency components of the C-V curve.

Fig. 11 demonstrates the effectiveness of the Savitzky-Golay filter for appropriately chosen filter parameters; measurements for a $W/L = 1.0\ \mu$m/0.1 μm PMOS device are used as an example. Even with an OSR of 2^{15}, the unfiltered data remains somewhat noisy. In comparison, using an OSR of 2^{11} and a filter with parameters set to $F = 61$ and $N = 3$ results in a low-noise measurement, which tracks the unfiltered data very well; the filter parameters are empirically adjusted to adequately suppress the high-frequency noise while at the same time retaining the underlying non-linear shape of the C-V curve. At an OSR of 2^{11}, a 256-point C-V measurement takes only 45 sec to complete, making the acquisition of large statistical data sets feasible.

IV. Measurement Results

Two identical copies of the measurement circuitry described in Section II are implemented on the same 45-nm bulk CMOS chip (Fig. 12) using complete back-end metallization consisting of 7 interconnect layers. One copy is used to characterize NMOS devices, while the other is used to characterize PMOS devices; both copies are operated in parallel for increased measurement throughput. While the two copies of the system are identical in their design, their analog references and internal controls are set up to accommodate NMOS and PMOS current polarities, respectively. The majority of the chip area is occupied by the DUT arrays, with the DAC and MU circuitry integrated in the periphery of the test chip.

A. System Characterization

Table I summarizes the measured performance of the R-string DAC and the current- and voltage-mode ADC. The DAC operates at sampling rates of up to 2 MHz at an 8-bit resolution with a $V_{\rm LSB}$ of 4.3 mV. The current-mode ADC is configured with $I_{\rm REF} = 10\ \mu$A and $N_{\rm REF} = 1024$ for an $I_{\rm LSB}$ of 9.76 nA with a 12-bit resolution at a variable sampling rate of 75–200 kHz. The voltage-mode ADC is configured with $V_{\rm REF} = 1.5$ V and

TABLE I
MEASURED CONVERTER PERFORMANCE

Conv. Type	Res.	Samp. Freq.	LSB	max. DNL	max. INL
DAC	8-bit	2 MHz	4.3 mV	0.1 LSB	0.1 LSB
I-mode ADC	12-bit	75 kHz-200 kHz	9.76 nA	0.3 LSB	0.6 LSB
V-mode ADC	10-bit	75 kHz-200 kHz	0.976 mV	0.1 LSB	0.3 LSB

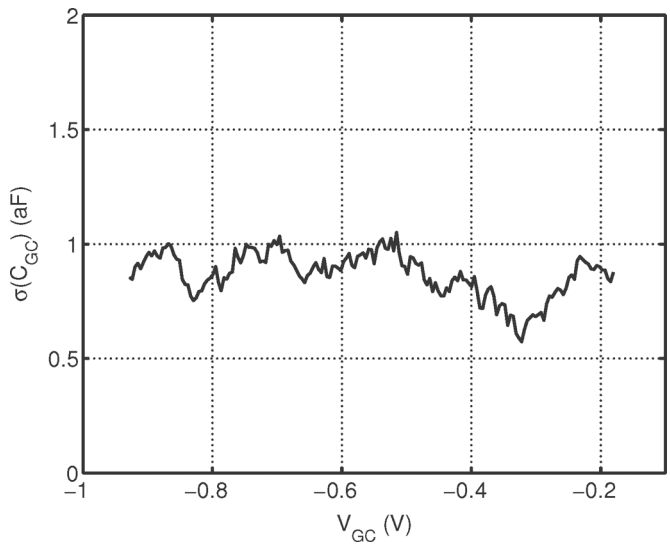


Fig. 13. Standard deviation of 16 repeated measurements of C_{GC} across bias; the curve demonstrates the excellent reproducibility of the capacitance measurement.

$N_{\mathrm{REF}} = 1024$ for a V_{LSB} of 0.976 mV with a 10-bit resolution at a variable sampling rate of 75–200 kHz. All analog references for the data converters are supplied externally and there is no need for additional calibration to achieve the reported resolution specifications.

When the system operates in C-V mode, I_{LSB} is reduced to 390.6 pA, and additional oversampling and filtering is used as described in Section III. To estimate the achieved measurement precision we examine the measurement reproducibility. Fig. 13 shows deviation from the mean of a PMOS C-V measurement across the entire bias range of interest. The standard deviation is taken across 16 identical measurements per bias point. The maximum observed standard deviation is 1.05 aF with mean standard deviation across all bias points of 0.87 aF.

B. Combined C-V/I-V Measurements and Parameter Extraction

Figs. 14 and 15 show constellation plots of I_D as a function of V_{GS} for $V_{DS} = 60$ mV, and C_{GC} as a function of V_{GC}, respectively. Fifteen different DUT types, spanning the space of $W = [0.2 - 1.0]$ μm and $L = [0.04 - 0.11]$ μm, are measured across four chips, yielding 312 unique measurements per device type. The data contain measurements of both NMOS and PMOS devices, allowing comparisons to be drawn between the two device polarities. More importantly, I-V and C-V data are measured for the exact same device, allowing correlations between these measurements to be observed.

While the versatility of the combined C-V/I-V measurement approach makes it possible to analyze variability in practically any parameter governing the quasi-static transistor behavior, the analysis presented in this work focuses on variability in the small-signal transconductance, G_M, and the intrinsic gate-to-channel capacitance, $C_{GC,int}$. In particular, I-V data are used to extract G_M as given by

$$G_M(V_{GS}) \equiv \frac{\partial I_D}{\partial V_{GS}}. \tag{7}$$

In order to suppress the effect of threshold-voltage variation, G_M is observed at an overdrive voltage, $V_{GS} - V_{T,lin} = 200$ mV, where $V_{T,lin}$ is the the linear threshold voltage extracted for each DUT using the extrapolation-in-the-linear-region (ELR) method [20]. On the other hand, C-V data are used to extract variability in $C_{GC,int}$; $C_{GC,int}$ is approximated by the difference in C_{GC} measured at high and low bias.

C. Random Variability

All random parameter fluctuations are analyzed by considering the difference in the parameter of interest extracted from two matched DUTs in the DUT array. This difference is given by

$$\Delta P = P_1 - P_2 \tag{8}$$

where P_1 and P_2 are the extracted parameter values for the two matched DUTs. Such a pseudo-differential measurement approach cancels out the effects of any systematic parameter gradients along the columns of the DUT array. Within-die random variation is assumed to be the same across all measured chips. Gathering measurement data from four chips results in 156 differential parameter measurements, which is the sample size used in all random variability analysis presented in this work.

1) G_M Variability: When studying the variability in G_M, the following model for the drain current, I_D, when the device is biased in the triode region with $V_{DS} = 50$ mV, is assumed:

$$I_D = k\frac{W}{L_{\mathrm{eff}}}(V_{GS} - V_{T,\mathrm{lin}})V_{DS} \tag{9}$$

where k is the product of the effective channel mobility, μ_{eff}, and oxide capacitance per unit area, C'_{ox}. Therefore, by the definition in (7), G_M is given by

$$G_M(V_{GS}) \equiv \frac{\partial I_D}{\partial V_{GS}} = k\frac{W}{L_{\mathrm{eff}}}V_{DS} \tag{10}$$

To study the relative variability in $(\Delta G_M)/(G_M)$, the effects of the variance of W, L_{eff}, and k can be propagated, as described in [21]. In particular, the variance of $(\Delta G_M)/(G_M)$ is given by

$$\sigma^2_{\Delta G_M/G_M} = \left(\frac{\partial \frac{\Delta G_M}{G_M}}{\partial \Delta L}\right)^2 \sigma^2_{\Delta L} + \left(\frac{\partial \frac{\Delta G_M}{G_M}}{\partial \Delta W}\right)^2 \sigma^2_{\Delta W} + \left(\frac{\partial \frac{\Delta G_M}{G_M}}{\partial \frac{\Delta k}{k}}\right)^2 \sigma^2_{\Delta k/k}, \tag{11}$$

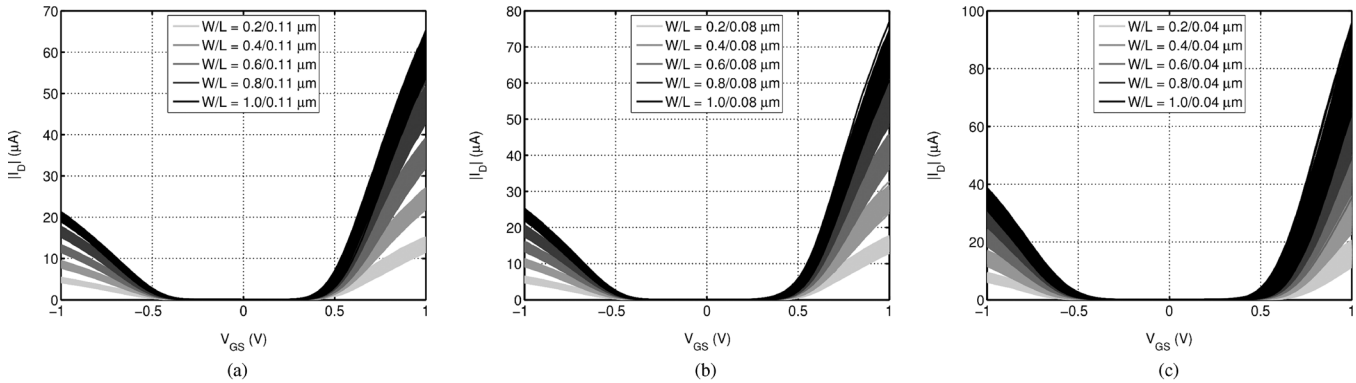


Fig. 14. PMOS (negative V_{GC}) and NMOS (positive V_{GC}) I-V measurements across four different test chips. (a) $L = 0.11\ \mu$m, (b) $L = 0.08\ \mu$m, (c) $L = 0.04\ \mu$m.

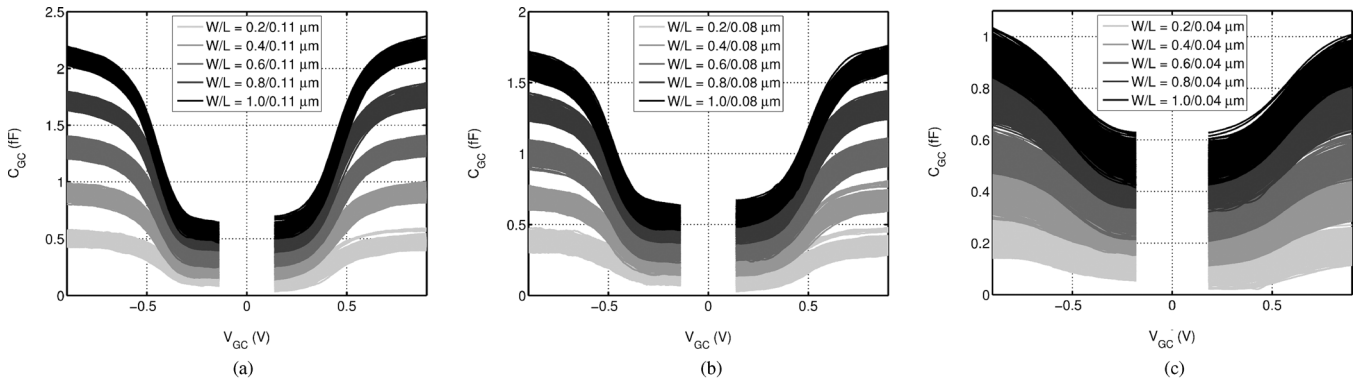


Fig. 15. PMOS (negative V_{GC}) and NMOS (positive V_{GC}) C-V measurements corresponding to the I-V measurements in Fig. 14. (a) $L = 0.11\ \mu$m, (b) $L = 0.08\ \mu$m, (c) $L = 0.04\ \mu$m.

TABLE II
EXTRACTED VALUES OF $A_{\Delta L}$, $A_{\Delta W}$, AND $A_{\Delta k/k}$ FROM (16)

Parameter	NMOS	PMOS
$A_{\Delta L}$ $(\mu m^{3/2})$	0.4×10^{-3}	0.5×10^{-3}
CI	$[0 - 1.1] \times 10^{-3}$	$[0.3 - 0.8] \times 10^{-3}$
$A_{\Delta W}$ $(\mu m^{3/2})$	2.0×10^{-3}	0.6×10^{-3}
CI	$[1.1 - 2.9] \times 10^{-3}$	$[0 - 2.1] \times 10^{-3}$
$A_{\Delta k/k}$ (μm)	8.2×10^{-3}	6.8×10^{-3}
CI	$[7.1 - 9.3] \times 10^{-3}$	$[6.1 - 7.5] \times 10^{-3}$

where

$$\sigma^2_{\Delta L} = \frac{A^2_{\Delta L}}{W}, \tag{12}$$

$$\sigma^2_{\Delta W} = \frac{A^2_{\Delta W}}{L_{\text{eff}}}, \tag{13}$$

and

$$\sigma^2_{\Delta k/k} = \frac{A^2_{\Delta k/k}}{W L_{\text{eff}}}. \tag{14}$$

The partial derivatives in (11) can be derived from (10) as follows:

$$\frac{\partial \frac{\Delta G_M}{G_M}}{\partial \Delta L} \approx \frac{1}{L_{\text{eff}}}$$
$$\frac{\partial \frac{\Delta G_M}{G_M}}{\partial \Delta W} = \frac{1}{W}$$
$$\frac{\partial \frac{\Delta G_M}{G_M}}{\partial \frac{\Delta k}{k}} = 1. \tag{15}$$

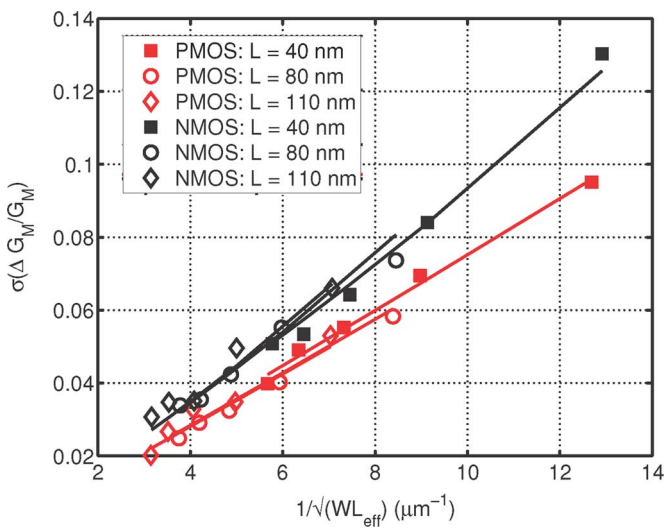


Fig. 16. Pelgrom plot of $\sigma_{\Delta G_M/G_M}$ against the inverse square root of effective device area, $1/\sqrt{WL_{\text{eff}}}$; solid lines represent a fit to (16).

Plugging (12), (13), (14), and (15) into (11) results in

$$\sigma^2_{\Delta G_M/G_M} = \frac{A^2_{\Delta L}}{W L^2_{\text{eff}}} + \frac{A^2_{\Delta W}}{W^2 L_{\text{eff}}} + \frac{A^2_{\Delta k/k}}{W L_{\text{eff}}}. \tag{16}$$

Fig. 16 shows a Pelgrom plot [22] of the measured standard deviation of the relative transconductance, $\sigma^2_{\Delta G_M/G_M}$, for both NMOS and PMOS devices across the span of W and L_{eff}. Solid lines represent a fit to (16), and the extracted parameters along with their 95% confidence intervals are listed in Table II. While

the variability in k accounts for most of the G_M variability in either device type, values for $A_{\Delta L}$ and $A_{\Delta W}$ are also extracted. Extracting values for these two parameters is important, as it gives an indication of the amount of line-edge roughness (LER) present in the technology. However, due to the dominance of the $A_{\Delta k/k}$ term, the uncertainty in determining the LER parameters is too large.

It is interesting to note that the $A_{\Delta k/k}$ term for PMOS transistors, and consequently, the overall $\sigma_{\Delta G_M/G_M}$, is less than that for NMOS transistors in this technology, even as the higher μ_{eff} and slightly higher C'_{ox} of the NMOS transistors result in a higher value for k and should tend to decrease $\sigma_{\Delta k/k}$. If it is assumed that variations in μ_{eff} dominate variations in k, then the data presented in Fig. 16 indicate that the mobility in the PMOS channel is better controlled. This could be related to the fact that different strain techniques are used to boost the mobility in the NMOS and PMOS channels. It is possible that the compressive strain, used in PMOS devices, is better controlled than tensile stress, used in NMOS devices. Additionally, Coulomb scattering is expected to give rise to more μ_{eff} variability in NMOS devices as compared to PMOS devices due to the comparatively larger random dopant fluctuation (RDF), as observed in [23], where the annealing process has been shown to result in a comparative increase in NMOS dopant fluctuations due to defect migration.

2) $C_{GC,\text{int}}$ Variability: Similarly to the treatment of the variability in G_M described above, propagation of variance can be used to gain a better understanding of the causes of variability in the intrinsic gate-to-channel capacitance, $C_{GC,\text{int}}$. Neglecting the effects of the inner fringe capacitance, the intrinsic gate capacitance can be approximated by the difference in the measured C_{GC} in inversion and depletion (high and low $|V_{GS}|$ bias, respectively), and is given by

$$C_{GC,\text{int}} \approx C'_{ox} W L_{\text{eff}}, \tag{17}$$

where W and L_{eff} represent the effective dimensions of the device, and C'_{ox} represents the oxide capacitance per unit area. Applying propagation of variance gives

$$\begin{aligned}\sigma^2_{\Delta C_{GC,\text{int}}} \approx & \left(\frac{\partial \Delta C_{GC,\text{int}}}{\partial \Delta L}\right)^2 \sigma^2_{\Delta L} \\ & + \left(\frac{\partial \Delta C_{GC,\text{int}}}{\partial \Delta W}\right)^2 \sigma^2_{\Delta W} \\ & + \left(\frac{\partial \Delta C_{GC,\text{int}}}{\partial \Delta C'_{ox}}\right)^2 \sigma^2_{\Delta C'_{ox}},\end{aligned} \tag{18}$$

where

$$\sigma^2_{\Delta C'_{ox}} = \frac{A^2_{\Delta C'_{ox}}}{W L_{\text{eff}}}, \tag{19}$$

and $\sigma^2_{\Delta L}$ and $\sigma^2_{\Delta W}$ are given by (12) and (13), respectively. Plugging in (17), (19), (12), and (13) into (18), the expression

$$\frac{\sigma^2_{\Delta C_{GC,\text{int}}}}{C'^2_{ox}} \approx A^2_{\Delta L} W + A^2_{\Delta W} L_{\text{eff}} + A^2_{\Delta C'_{ox}/C'_{ox}} W L_{\text{eff}} \tag{20}$$

is derived, where

$$A_{\Delta C'_{ox}/C'_{ox}} = \frac{A_{\Delta C'_{ox}}}{C'_{ox}}. \tag{21}$$

It should be noted that this expression allows the extraction of the LER parameters $A_{\Delta L}$ and $A_{\Delta W}$, as well as the relative variance of the oxide capacitance per unit area given by

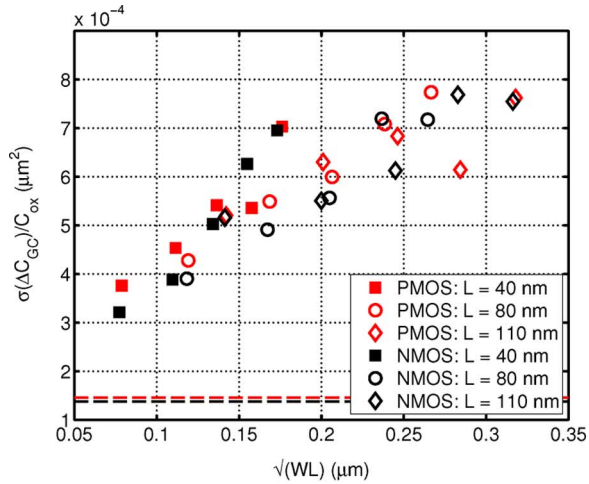
$$\sigma^2_{\Delta C'_{ox}/C'_{ox}} = \frac{A^2_{\Delta C'_{ox}/C'_{ox}}}{W L_{\text{eff}}}. \tag{22}$$

All of these parameters are also present in the treatment of $\sigma_{\Delta G_M/G_M}$ discussed above. The ability to extract and compare variability in physical device parameters from both C-V and I-V data is uniquely enabled by the combined C-V/I-V characterization methodology described in this work.

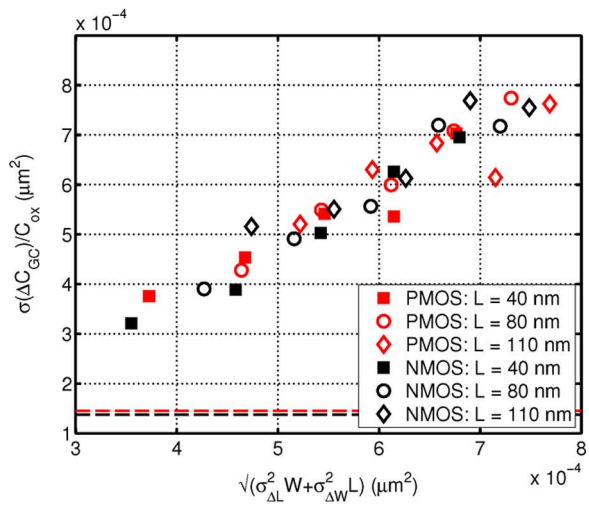
In the process of fitting the measured $C_{GC,\text{int}}$ variability data to the model shown in (20), it is found that the $\sigma^2_{\Delta C'_{ox}/C'_{ox}}$ term does not contribute at a statistically significant level and can be ignored in the case of both NMOS and PMOS data analysis. This result points to the fact that the major source of variation in gate-to-channel capacitance matching is not traced back to variations in C'_{ox}, but to variations in the effective dimensions of the device instead. Such a conclusion is logical, as the variations studied are very localized due to the proximity of the matched DUTs, and the gate oxide film is not expected to vary significantly over a small distance. Unlike the case of $\sigma_{\Delta G_M/G_M}$, where variations in the parameter k account for most of the measured variability, in the case of $\sigma_{\Delta C_{GC,\text{int}}}$ essentially all of the variability comes from $\sigma_{\Delta L}$ and $\sigma_{\Delta W}$. Consequently, analyzing $\sigma_{\Delta C_{GC,\text{int}}}$ proves to be a much more effective way of extracting the variation in device geometry due to LER.

Fig. 17 shows $(\sigma_{\Delta C_{GC,\text{int}}})/(C'_{ox})$ plotted against the effective device area, $\sqrt{W L_{\text{eff}}}$, as well as against $\sqrt{A^2_{\Delta L} W + A^2_{\Delta W} L_{\text{eff}}}$. The former is equivalent to a classical Pelgrom treatment of $\sigma_{\Delta C_{GC,\text{int}}/C_{GC,\text{int}}}$ modeled as proportional to $(1)/(\sqrt{W L_{\text{eff}}})$; such an interpretation of the measured variability in $C_{GC,\text{int}}$ across geometry is presented in [17], but even there the data reported fails to give an accurate fit to the basic Pelgrom expression. On the other hand, a much better alignment between data from minimum-length devices and the rest of the DUT parameter space is seen in Fig. 17(b), where only the perimeter effects due to LER are considered.

The extracted data are fairly noisy, as the standard deviations measured are close to the overall measurement precision, marked with dashed lines in Fig. 17. However, due to the large number of points, $A_{\Delta L}$ and $A_{\Delta W}$ can be extracted fairly precisely, as shown in Table III. A comparison between the values in Tables III and II shows that the mean LER parameters extracted using the $C_{GC,\text{int}}$ variability data fall within the confidence interval of those extracted using the G_M variability data, but with much higher precision as evidenced by the tighter confidence intervals. It is interesting to note that L_{eff} is controlled about twice as well as W. Attention is put into controlling the length of the device, as variations in L_{eff} have a higher impact on overall device performance. Additionally, the fact that $(\sigma^2_{\Delta C_{GC,\text{int}}})/(C'^2_{ox})$ is insensitive to $\sigma^2_{\Delta C'_{ox}/C'_{ox}}$ implies that variations in μ_{eff} are the primary source of variation in $(\Delta k)/(k)$, consistent with the discussion of variation in G_M.



(a)



(b)

Fig. 17. $(\sigma_{\Delta C_{GC,\mathrm{int}}})/(C'_{ox})$ (a) as a function of $\sqrt{WL_{\mathrm{eff}}}$, and (b) taking LER into account; modeling $(\sigma_{\Delta C_{GC,\mathrm{int}}})/(C'_{ox})$ as dependent on the device perimeter rather then the device area aligns minimum-length device data (filled squares) with the rest of the measurements; dashed lines indicate the C-V measurement noise floor, conservatively defined as twice the maximum measured error in Fig. 13.

TABLE III
EXTRACTED VALUES OF $A_{\Delta L}$ AND $A_{\Delta W}$ FROM (20)

Parameter	NMOS	PMOS
$A_{\Delta L}$ $(\mu m^{3/2})$	0.6×10^{-3}	0.6×10^{-3}
CI	$[0.5 - 0.7] \times 10^{-3}$	$[0.5 - 0.7] \times 10^{-3}$
$A_{\Delta W}$ $(\mu m^{3/2})$	1.1×10^{-3}	1.3×10^{-3}
CI	$[0.8 - 1.5] \times 10^{-3}$	$[0.9 - 1.8] \times 10^{-3}$

D. Systematic Variability

Another aspect of device variability, which can be studied using the proposed combined C-V/I-V characterization methodology, is systematic variability across the die. Up to this point, all analysis we have described is based on modeling the matching of parameters, as described by (8), canceling out the effects of systematic variability in order to focus on random variability instead. However, systematic variability can also be studied, by extracting parameter gradients across the die. Such gradients are not random in nature, and as such, do not scale with the area or the perimeter of the device; instead, they can be traced to a systematic source which affects all devices in a similar manner independent of their geometry.

In order to examine parameter gradients across the DUT array, each parameter of interest is measured, and then measurements along a column of the chip are normalized according to

$$\mathbf{P}_n = \frac{\mathbf{P} - \mu(\mathbf{P})}{\sigma(\mathbf{P})} \tag{23}$$

where $\mathbf{P}$ is a vector of extracted parameter values along the length of one column, $\mu(\mathbf{P})$ is its mean value, $\sigma(\mathbf{P})$ is its standard deviation, and $\mathbf{P}_n$ is the resulting normalized parameter vector. Using this type of normalization enables the study of gradient vectors along a DUT array consisting of different types of DUTs.

Heat maps for extracted normalized gradients of $C_{GC,\mathrm{int}}$ across the DUT array for both NMOS and PMOS devices are shown in top-left and top-right of Fig. 18, respectively. A well-defined gradient is observed, which points to a systematic source of variation in the intrinsic gate-to-source capacitance. This source of variation appears to be common to both NMOS and PMOS devices, as indicated by a correlation coefficient between the two measurements of $\rho = 0.91$.

If gradients in the normalized small-signal transconductance, G_M, are considered, similar patterns emerge, as seen in bottom-left and bottom-right of Fig. 18. Interestingly, the gradients in the normalized $C_{GC,\mathrm{int}}$ and normalized G_M exhibit strong negative correlation, with correlation coefficients of $\rho = -0.66$ and $\rho = -0.82$ in the case of PMOS and NMOS measurements, respectively.

When considering the functional form of $C_{GC,\mathrm{int}}$ shown in (17) and that of G_M shown in (10), it is clear that the only inverse correspondence between the two is through the effective device length, L_{eff}. Therefore, by leveraging the combined C-V/I-V characterization approach, the source of the negatively-correlated systematic variation in the two parameters is identified as a systematic variation in the length of the device, L. Since similar gradients are present in all measured dice, this systematic error can be traced to a lithographical or mask-alignment issue. Systematic variations of device length across the reticle are also reported in [24]. It should be noted that the gradients detected in $C_{GC,\mathrm{int}}$ are much smoother than those in G_M, due to the fact that the latter set of measurements is obscured by a relatively high variation in μ_{eff} on top of the underlying systematic length variation. This once again demonstrates the benefit of studying variation in the gate-to-channel capacitance, as it gives a much cleaner representation of variations in the intrinsic device geometry.

V. CONCLUSION

An on-chip combined C-V/I-V characterization system with digital interfaces has been presented. The system has been implemented in a 45-nm CMOS process, demonstrating 9.76-nA resolution current measurements, sub-1-mV resolution voltage measurements, and single aF resolution capacitance measurements of large statistical sets of circuit-representative NMOS and PMOS devices. Variation in the gate capacitance, C_{GC}, at circuit-representative device sizes has been shown to be dominated by variations in L and W, rather than C'_{ox}. Based on

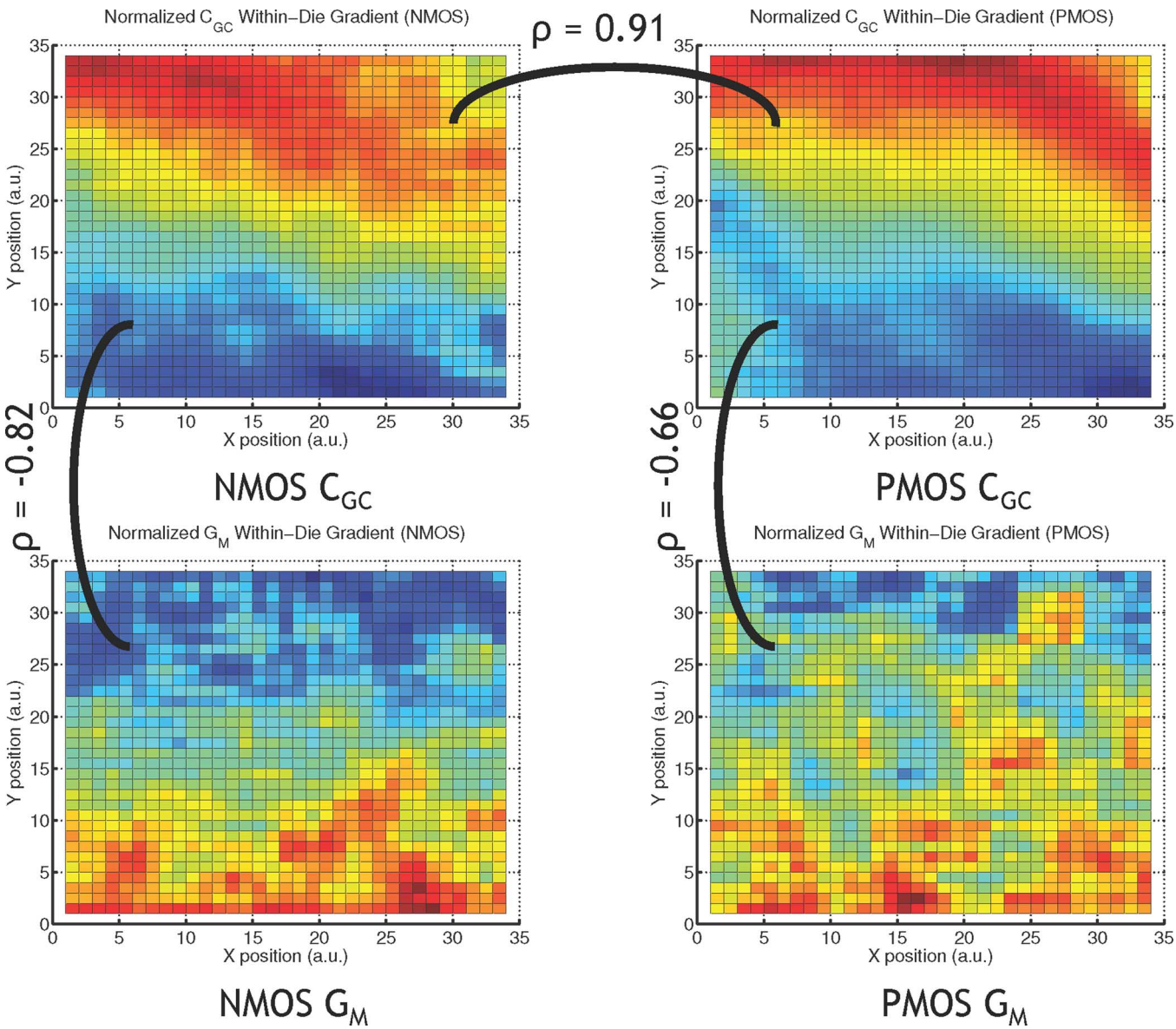


Fig. 18. Normalized gradients in C_{GC} across the die for (top-left) NMOS (top-right) PMOS devices and corresponding normalized gradients in G_M across the same die for (bottom-left) NMOS (bottom-right) PMOS devices; correlation between the measured is annotated.

this realization, the LER variability parameters, $\sigma_{\Delta L}$ and $\sigma_{\Delta W}$, have been extracted from C_{GC} variability data. A proposed combined C-V/I-V characterization approach has been successfully used to identify variations in μ_{eff} as the primary source in relative variations in the small-signal transconductance, G_M, as well as a systematic shift in L as the reason behind well-defined gradients across the die, affecting both G_M and C_{GC}. While the work presented here is complete, it should be noted that the variability analysis described is only one example of the kind of analysis that is made possible by using the on-chip combined C-V/I-V characterization system, with many other possibilities for analysis open.

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Simeon Realov (M'12) received the B.S. degree in engineering from Swarthmore College, Swarthmore, PA, USA, in 2006 and the M.S. and Ph.D. degrees in electrical engineering from Columbia University, New York, NY, USA, in 2007 and 2012, respectively.

During his time at Columbia University, he worked on various methods for detailed on-chip device characterization and statistical modeling of device variability in advanced CMOS processes. He held several internship positions at IBM T. J. Watson Research Center, Yorktown Heights, NY, USA, where he developed techniques for on-chip capacitance measurement, combined C-V/I-V transistor characterization, as well as a fully-integrated SRAM fluctuations monitoring circuit. He also held a summer internship position with Rambus, Inc., Sunnyvale, CA, USA, where he worked on the design of a high-bandwidth on-chip supply noise monitoring system. After his graduation from Columbia University in 2012, he joined Intel Corporation, Hillsboro, OR, USA, where he is currently a member of the Digital Circuits and Library group working on standard cell design.

Kenneth L. Shepard (M'91–SM'03–F'08) received the B.S.E. degree from Princeton University, Princeton, NJ, USA, in 1987 and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, USA, in 1988 and 1992, respectively.

From 1992 to 1997, he was a Research Staff Member and Manager with the VLSI Design Department, IBM T. J. Watson Research Center, Yorktown Heights, NY, USA, where he was responsible for the design methodology for IBMs G4 S/390 microprocessors. Since 1997, he has been with Columbia University, New York, NY, USA, where he is now a Professor of electrical engineering and biomedical engineering. He also was Chief Technology Officer of CadMOS Design Technology, San Jose, CA, USA, until its acquisition by Cadence Design Systems in 2001. His current research interests include power electronics, carbon-based devices and circuits, and CMOS bioelectronics.

Dr. Shepard was Technical Program Chair and General Chair for the 2002 and 2003 International Conference on Computer Design, respectively. He has served on the Program Committees for IEDM, ISSCC, VLSI Symposium, ICCAD, DAC, ISCAS, ISQED, GLS-VLSI, TAU, and ICCD. He received the Fannie and John Hertz Foundation Doctoral Thesis Prize in 1992, a National Science Foundation CAREER Award in 1998, and the 1999 Distinguished Faculty Teaching Award from the Columbia Engineering School Alumni Association. He has been an Associate Editor of IEEE TRANSACTIONS ON VERY LARGE-SCALE INTEGRATION (VLSI) SYSTEMS and is currently an Associate Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS and IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS.