INVITED PAPER

Graphene Field-Effect Transistors Based on Boron–Nitride Dielectrics

In this paper, the authors explore the use of hexagonal boron nitride as a dielectric material in graphene devices. They show that the performance of such devices is considerably improved compared to the ones using conventional dielectrics.

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ABSTRACT | Two-dimensional atomic sheets of graphene represent a new class of nanoscale materials with potential applications in electronics. However, exploiting the intrinsic characteristics of graphene devices has been problematic due to impurities and disorder in the surrounding dielectric and graphene/dielectric interfaces. Recent advancements in fabricating graphene heterostructures by alternately layering graphene with crystalline hexagonal boron nitride (hBN), its insulating isomorph, have led to an order of magnitude improvement in graphene device quality. Here, recent developments in graphene devices utilizing boron–nitride dielectrics are reviewed. Field-effect transistor (FET) characteristics of these systems at high bias are examined. Additionally, existing challenges in material synthesis and fabrication and the potential of graphene/BN heterostructures for novel electronic applications are discussed.

KEYWORDS | Graphene field-effect transistors (GFETs); hexagonal boron nitride (hBN)

I. INTRODUCTION

For the past several decades, aggressive scaling of silicon-based technologies has enabled a steady exponential growth in semiconductor device performance, following the predications of Moore's law. Further device scaling cannot continue indefinitely, and it is predicted that in only a few years a fundamental small-scale limit in device architecture will be reached. This rapidly approaching end has animated an intensive search for novel channel materials that can outperform state-of-the-art silicon. Among these, graphene, a 2-D sheet of carbon atoms arranged in a honeycomb lattice, has attracted significant attention. Its atomically thin structure, high mechanical strength, high mechanical flexibility, high thermal conductivity, optical transparency, and potential low cost, in conjunction with its superior intrinsic carrier velocities, has made graphene attractive as a promising new material for a wide range of applications [1]–[5].

The 2-D nature of graphene means that injected charge carriers are confined to a surface just one atom thick (~0.3 nm). In principal, this alone may allow graphene-based devices to push the limits of device scaling beyond those of silicon by enabling improved gate control and, therefore, reduced short channel effects in ultrashort channel devices. However, the extreme confinement means that charge carriers are also directly exposed to the surrounding environment, making transport through graphene highly sensitive to scattering from extrinsic impurities. This sensitivity has presented a serious

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engineering challenge to realizing high-performance devices that take full advantage of graphene's intrinsic qualities.

Graphene has no native oxide layer and instead presents a chemically inert surface with no open bonds, making it difficult to integrate dielectric passivation without chemically altering the graphene surface and degrading the transport properties of the graphene channel. The fundamental challenge in the development of graphene field-effect transistors (GFETs) has, therefore, been engineering a dielectric interface that provides optimal capacitive coupling to the gate, while also minimizing degradation of device performance.

In an effort to meet these challenges, hexagonal boron nitride (hBN) has emerged as an exceptional dielectric for GFET application. hBN is a wide bandgap semiconductor (5.97 eV) [6], sharing the same layered-hexagonal crystal structure as graphite but with boron and nitrogen atoms occupying the A and B sublattices in the Bernal structure. The strong in-plane bonding of the hexagonal structure (with only 1.7% lattice mismatch to graphene [7]) makes the surface free of dangling bonds and, thus, chemically inert, presenting a nearly ideal dielectric interface to graphene (Fig. 1). Indeed, devices fabricated on hBN substrates are found to exhibit an order-of-magnitude improvement in device mobility, reduced carrier inhomogeneity, lower extrinsic doping, reduced chemical reactivity, and improved high-bias performance in comparison to devices fabricated with conventional oxide dielectrics. The dielectric properties of hBN ($\epsilon \sim 4$ and $V_{\text{Breakdown}} \sim 0.7$ V/nm) compare favorably with SiO_2 [8], [9], and the excellent thermal conductivity of hBN [10], 600-times higher than silicon dioxide, is advantageous for FET applications to improve heat dissipation.

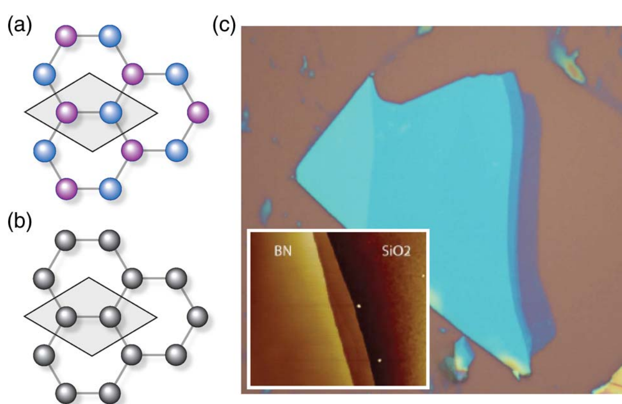


Fig. 1. ***(a) hBN and (b) graphene share the same lattice structure with boron and nitrogen replacing the carbon atoms in the unit cell (the unit cell is highlighted in each by the shaded region). (c) An optical micrograph of an exfoliated hBN sample on SiO_2. Inset shows an AFM image of a similar flake, showing the smooth single crystalline hBN surface. While the texture of the SiO_2 surface is visibly apparent, the hBN is approximately three times less rough.***

In this paper, we review the latest developments in layered graphene/hBN heterostructures and discuss the role that this improved dielectric is expected to play in enabling high-frequency analog GFET applications. We begin by first reviewing the state-of-the-art GFETs fabricated with conventional oxide dielectrics, demonstrating the shortcomings of these dielectrics in conjunction with graphene. Next, we review recently developed techniques that have enabled fabrication of graphene/hBN structures without the need for conventional oxide dielectrics. We then review direct current (dc) measurements of hBN supported GFETs with particular emphasis on the improved transistor current-voltage characteristics observed in short-channel devices. We compare RF measurements performed on hBN-supported structures with high-frequency devices fabricated with conventional dielectrics. We then discuss the possible role a bandgap may play in improving RF performance. Finally, we outline the current status of extending the fabrication of high-performance graphene FETs and graphene-based heterostructure FETs to the wafer scale.

II. GRAPHENE TRANSISTORS BASED ON CONVENTIONAL OXIDE DIELECTRICS

Graphene bandstructure is characterized by a linear dispersion near the symmetry points where the valence and conduction bands touch. At the charge neutrality point (CNP), where the bands cross, local impurities form an inhomogeneous network of spatially segregated electron and hole puddles. Therefore, even in undoped graphene, these potential fluctuations result in residual conduction paths, which limit the achievable minimum conductivity at the CNP. At ambient temperatures, this inhomogeneous charge network is "smeared out" giving rise to a sizable minimum conductivity at the CNP. This limits the ON/OFF current ratio achievable in graphene to the order of 10 in the cleanest devices, making graphene impractical for use in digital applications where typical ON/OFF ratios of greater than 10^4 are desired for logic operation [11]. For intrinsic graphene, where room temperature transport is limited only by scattering off of internal phonon modes, the electron drift velocity is predicted to be greater than 4×10^7 cm/s [12], nearly four times larger than in Si. The main interest in graphene electronics, therefore, lies in high-frequency analog transistor applications where a bandgap is not required and the short transit times could enable power gain at frequencies exceeding 1 THz [13], [14].

GFET devices are typically fabricated on SiO_2-supported graphene. Alternative substrates such as SiC [16] have been utilized; however, in all cases, a local gate is required for high-bias operation. In order to accomplish this, an oxide dielectric is typically deposited onto the top surface of the graphene sheet followed by evaporation of a top metal gate [Fig. 2(a)]. The top-gate dielectric requires

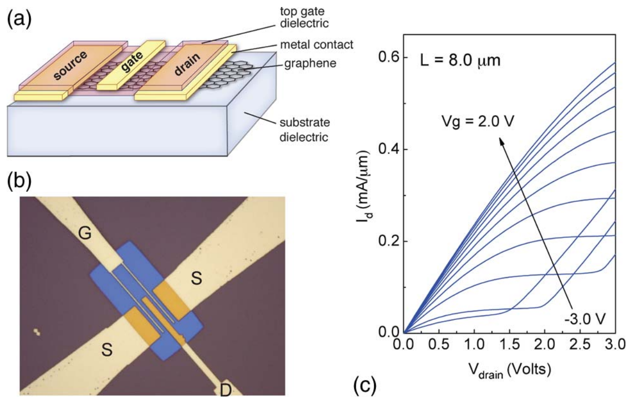


Fig. 2. ***(a) Schematic of a generic GFET construction. Typically, an oxide layer is deposited onto the top graphene surface to enable deposition of a local top gate. (b) An optical micrograph of a GFET fabricated in a π-gate structure to allow high-frequency characterization similar to [15]. (c) I–V characteristics of a 8-μm-long GFET showing current saturation and the characteristic "kink."***

an initial deposition of a noncovalent functionalization layer adsorbed on the graphene surface, such as a thin layer of oxidized aluminum or a polymer layer [17]–[19] in order to promote adhesion. In these devices, performance is limited not by the graphene itself, but rather by the chemically active buffer layer and oxide surfaces which trap charged impurities at the graphene interfaces, introduce dopants and Coulomb scatterers, impart roughness to the graphene sheet, and ultimately limit transport mobility and produce hysteretic current-voltage characteristics.

Despite these limitations, GFETs are shown to have respectable I–V characteristics at long channel lengths and impressive high-frequency performance at short channel lengths. Fig. 2(c) shows the typical saturating I–V characteristics of a 8-μm-long GFET associated with a unipolar channel. The observed current saturation is attributed to velocity saturation due to coupling to optical phonon modes. Under specific combinations of drain and gate biasing, the channel can be rendered ambipolar, resulting in a pronounced "kink" in the curves [21]. This is produced by the vanishing carrier density at the drain end as the CNP enters the channel with reduced gate-to-drain potential, rendering the current in the channel relatively insensitive to V_{drain}. By increasing the drain bias beyond the kink, the CNP moves further into the channel, and the opposite type of carriers is introduced into the channel from the drain. In this ambipolar regime, the CNP becomes a place of recombination for holes and electrons.

The radio-frequency (RF) performance of field-effect transistors (FETs) is usually quantified by the cutoff frequency f_T and the maximum oscillation frequency $f_{\max}$, which correspond to the frequencies at which the short-circuit current gain and maximum available power gain, respectively, roll off to unity. Intrinsic f_T (one that does not include the effects of device parasitics) is given by

$$f_T = \frac{g_m}{2\pi C_g} \tag{1}$$

where g_m is the transconductance and C_g is the gate capacitance. In the standard short-channel semiconductor model where current saturation at high source–drain bias results from saturation of the carrier velocity, leaves $f_T \propto v_{\mathrm{sat}}/L$, where v_{sat} is the saturation velocity and L is the channel length. For silicon complementary metal–oxide–semiconductor (CMOS), in which devices are scaled to the ballistic limit, this saturation velocity is determined by the carrier source injection velocity [22]. Maximizing f_T comes from enhancing v_{sat} and minimizing L. Indeed, intrinsic f_T values larger than 420 GHz for GFETs with conventional oxide dielectrics have been demonstrated by scaling the channel length to sub-100 nm [23]. However, RF measurements have generally been reported for top-gated device structures whose current-voltage characteristics do not show strong current saturation due to relatively poor gate–oxide interfaces or weak gate coupling [15], [16], [24]–[27]. As a result, device output conductance is high, power gain is limited, and the maximum oscillation frequency ($f_{\max}$) is typically only one-tenth of f_T [28].

$f_{\max}$ is generally the more important figure of merit for analog applications as power gain determines the ultimate utility of the device. $f_{\max}$ depends much more critically on certain parasitics such as gate resistance, and device characteristics, such as output resistance, than does f_T. $f_{\max}$ performance can be improved with device structures that show better current saturation and T-gate structures that reduce gate resistance.

Contact resistance directly degrades g_m and, therefore, has an effect on both f_T and $f_{\max}$. Realizing good contact resistance to graphene has long been problematic, with values reported in the literature ranging from $\sim$100 $\Omega\mu$m to more than 1 k$\Omega\mu$m. These values are 10–100 times larger than what is achieved in Si devices. Contact resistance effects become even more pronounced in short-channel devices as the relative contribution to the total device resistance increases.

While GFETs based on oxide dielectrics with device lengths of a few micrometers show good saturation, output resistance diminishes for devices scaled below a micrometer (Fig. 3). A recent study identified mobile trapped charges in these surrounding dielectrics as the reason behind the triode-like characteristics for short channel devices. Using a pulsed measurement approach to measure dc response on time scales shorter than the response time of the traps, full saturation is recovered in devices with channel lengths down to 140 nm [19]. Output

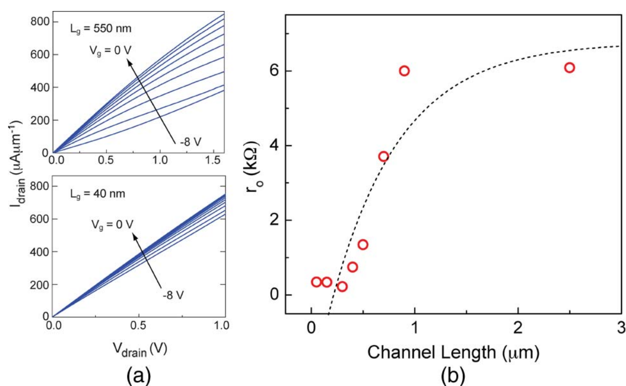


Fig. 3. ***Channel length scaling in GFETs fabricated with conventional oxide dielectrics. At short channel lengths, the high bias characteristics are substantially diminished, exhibiting practically no saturation for sub-100-nm devices. The two plots in (a) show I–V curves of devices fabricated from CVD-grown graphene with 550-nm (upper panel) and 40-nm (lower panel) gate lengths [20]. (b) Peak output resistance versus channel length measured from several exfoliated devices with a HfO_2 top gate dielectric (unpublished). Data are shown for the bias condition that results in the maximum output resistance. Dashed line is a guide to the eye highlighting the dramatic decrease in r_o at short channels.***

conductances as low as 0.3 mS/mm in saturation were reported, suggesting that an improved dielectric in these short channel GFETs could allow significant improvement in $f_{\max}$, and potentially eliminate the large discrepancy between $f_{\max}$ and f_T so far reported in the literature.

In spite of the impressive f_T values that have been achieved, the low mobility, low $f_{\max}$, and nonsaturating characteristics generally reported for GFETs with conventional oxide dielectrics raise significant questions as to whether graphene-based technologies can actually outperform silicon CMOS. A further concern is the importance of band-to-band Klein tunneling in very short channel GFETs, which may prevent current saturation even in the presence of improved dielectric interfaces [14]. The use of hBN dielectric with substantially improved interface to graphene provides an opportunity to address these questions.

III. GRAPHENE/hBN HETEROSTRUCTURES

A. Fabrication

The highest purity hBN currently available is synthetically grown using a high-pressure–high-temperature (HP–HT) method [29]. This results in millimeter-size crystallites, resembling flakes of Kish graphite, which can be exfoliated down to arbitrary thicknesses, using the same techniques that have been developed for producing graphene samples of an arbitrary number of layers [30]. Using a mechanical layer-by-layer fabrication process, GFETs can be built utilizing hBN as either the top or bottom layer dielectric (or both). This mechanical layering permits integration of uniform hBN layers with thicknesses down to a single monolayer, and without the need for the adhesion layer characteristic of oxide processes. Fig. 4 shows an example of the fabrication process flow we use to realize locally gated GFETs for high-bias dc operation, similar to the fabrication process developed in [31].

A false-colored scanning electron microscope (SEM) image of a device fabricated in this way is shown in Fig. 5. The device geometry shown here allows us to utilize the same hBN dielectric layer as both a supporting substrate and local-gate dielectric eliminating the need for an additional top gate. We note that this technique allows a variety of application-specific device architectures to be fabricated with only small variations to the process. For RF measurements, a two-finger (π)-gate layout is used to

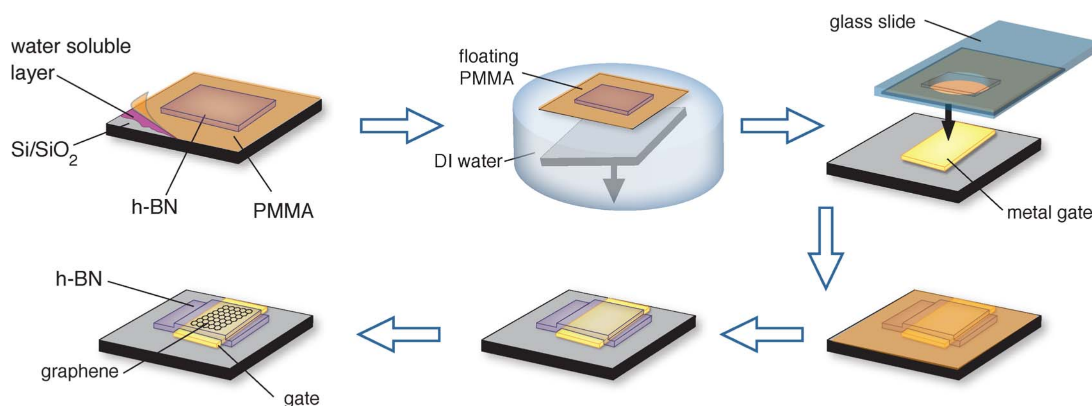


Fig. 4. ***The mechanical transfer of both graphene and hBN starts with exfoliated hBN on top of a Si chip with a two-layer polymer coating. The water soluble bottom polymer layer is dissolved in a water bath and the polymethyl methacrylate film with the hBN remains floating on the water surface. The hBN flake is transferred onto a predefined metal gate and the polymer layer dissolved, leaving the hBN on the metal. The same steps are repeated for graphene.***

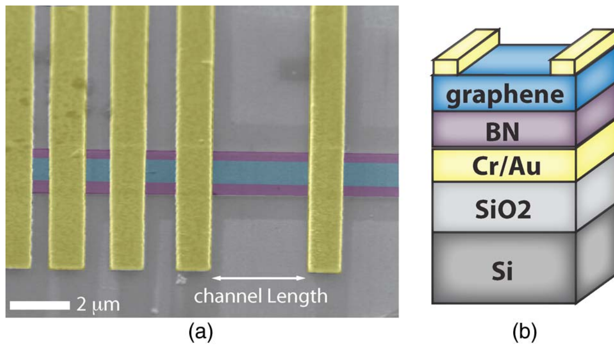


Fig. 5. *(a) False color SEM image showing a typical hBN-supported GFET device. (b) Cross-sectional schematic of the device shown in (a).*

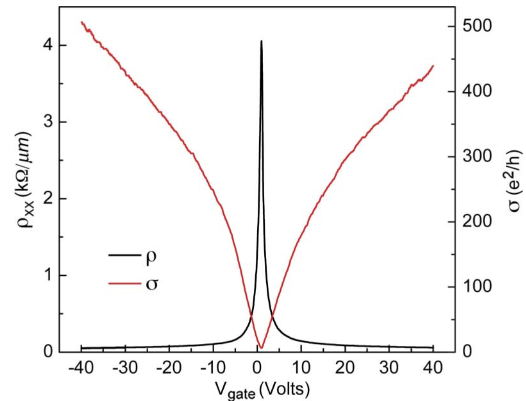


Fig. 6. *Resistivity (ρ) and conductivity (σ) as a function of gate voltage for a graphene Hall-bar device on hBN at 1.6 Kelvin. The conductivity has a sublinear behavior only observed in very high mobility samples. This represents an exceptional device, with the mobility measuring ~80 000 cm²/Vs at high density. The mean mobility measured from over 25 samples, at the same carrier density, measures ~35 000 cm²/Vs.*

allow *S*-parameter characterization at high frequencies with coplanar microprobes. To reduce gate resistance in the RF structure, 200-nm-thick tungsten metal gates are patterned into a 1-μm SiO_2 layer using a Damascene-like process, followed by a chemical–mechanical polishing (CMP) step to ensure a flat surface that exposes the gate metal surface [32].

B. DC Measurements

The first transport characteristics of a graphene/hBN device were reported for hBN supported heterostructures fabricated on Si/SiO_2 substrates, similar to that shown in Fig. 5, but utilizing a four-terminal Hall bar design and using the doped silicon substrate as a global bottom gate [31]. In Fig. 6, the four-probe resistivity and conductivity of such a device is shown. This device shows excellent transport by several measures. The charge neutrality point (Dirac voltage), manifested as a resistivity peak, is close to zero gate voltage and has a very narrow full width at half maximum, approximately 1 V, indicating nearly a full order of magnitude less inhomogeneity than usually measured in SiO_2-supported devices. The density-independent mobility extracted from the self-consistent Boltzmann equation [33] is approximately 80 000 cm^2/Vs, at least a factor of three better than in the best reported SiO_2-supported samples.

The improved transport of graphene/hBN heterostructures has recently also been confirmed by the measurement of ballistic transport in micrometer-long devices [35], measurement of improved temperature-dependent conductivity [38], and observation of disorder-limited physical phenomenon that previously were not observable in samples with conventional dielectrics [39], [40]. In addition, scanning tunneling microscope measurements show less inhomogeneity and surface roughness [36], [37].

The graphene/hBN FET devices also exhibit significantly enhanced high-bias characteristics [34], [41], [42], compared to GFETs fabricated with oxide dielectrics (as described in Section II) at comparable channel lengths. Using a local bottom-gated FET structure with multiple voltage probes along the length of the graphene (as shown in Fig. 5) allows the fabrication of different channel length devices out of the same sample. Fig. 7(a) shows the channel resistivity ρ at small source–drain bias (1 mV) as a function of the bottom-gate voltage $V_{\rm gate}$ for three devices with channel lengths of 3, 1, and 0.5 μm, measured at room temperature. The low-field mobility can be extracted from the two-probe measurements by $\mu = (1/C_g) * (L/W) * (g_m/V_{ds})$, where C_g is the gate capacitance, ~363 nF/cm^2 calculated from the measured hBN thickness of 8.5 nm. L and W are the device length and width, respectively, and g_m is the transconductance.

The mobility of the 3-μm device is close to 11 000 cm^2/Vs in ambient air, lower than typically reported for graphene-on-hBN Hall bar structures at cryogenic temperatures. Two-terminal measurements, however, consistently give lower mobilities when compared to four-terminal measurements, even of the same device, due to the large contribution of contact resistance to the total measured resistance. Furthermore, room temperature measurements are mostly limited by acoustic phonons, which freeze out and do not limit low-temperature transport. The CNP is at −0.07 V and the gate-voltage hysteresis is less than 10 mV, indicating that there is minimal doping of the graphene channel due to external impurities. hBN-supported devices appear to be more stable compared to other GFET types; they show unchanged characteristics after repeated measurements and demonstrate stability over the course of several months.

The I–V characteristics of three different channel length devices are shown in Fig. 7(b). All devices show current saturation as well as the kink associated with an ambipolar channel, as described in Section II. The 0.5-μm-channel-length device shows an $I_{\rm on}$ of more than 1 mA/μm. It is also important to consider the small-signal

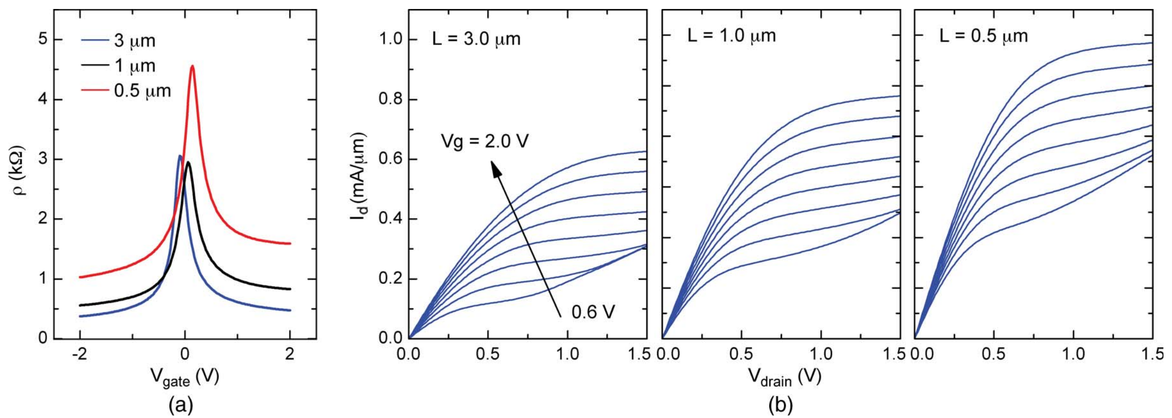


Fig. 7. ***DC measurements of GFETs in ambient conditions from [34]. (a) Low-field resistance of three devices with channel lengths of 3, 1, and 0.5 μm. (b) I–V characteristics of the same three devices for gate voltage from 0.6 to 2 V in 0.2-V steps.***

device parameters. The peak transconductance exceeds 400 mS/mm. The peak dc voltage gain $(g_m r_o)$ for this device is larger than 46, the highest value reported so far for any graphene FET [34]. Fig. 8 shows the maximum transconductance and the low-field mobility as a function of channel length. While g_m is relatively independent of channel length, the mobility of the devices drops by more than a factor of two as channel length decreases from 3 to 0.5 μm. Both the channel length independence of the transconductance and the change in mobility are consistent with velocity-saturation-dominated transport. The origin of the diminishing mobility with channel length is not presently understood, but this may be related to a combination of the increasing dominance of contact resistance at short channels and the difficulty in accurately determining mobility in this regime [43].

C. RF Measurements

Of particular importance for device applications, RF measurements recently conducted on GFETs exploiting high-quality boron–nitride dielectrics demonstrate improved power gain [41], [42]. The representative RF GFET device has a π-gate and a ground–signal–ground coplanar waveguide layout with a channel width of approximately 38 μm and channel length of 0.6 μm. The transconductance of this device is 280 mS/mm, somewhat lower than the devices described in Section III-B, mainly due to channel inhomogeneity more evident at large device widths. The high-frequency measurements shown in Fig. 9 are performed to 40 GHz with a standard open-short de-embedding method [44]. The current-gain (h_{21}) and unilateral power gain (U) are plotted at the bias point of peak g_m, yielding f_T and $f_{\max}$ of 44 and 34 GHz, respectively. Without de-embedding, f_T and $f_{\max}$ are 24 and 17 GHz, respectively.

Most importantly, the improved output characteristic of the hBN-supported GFETs enhances the unilateral power gain to a record value for graphene-based devices. In this relatively long-channel hBN-supported device,

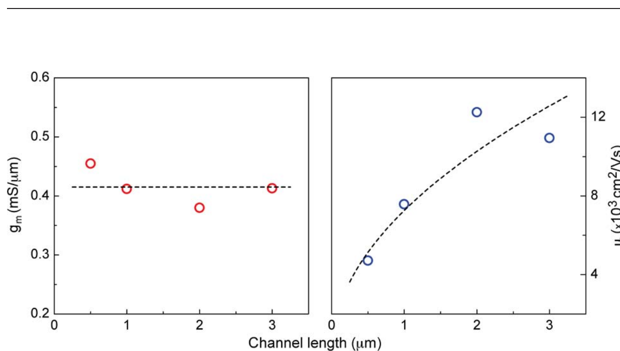


Fig. 8. ***Channel length dependence of g_m and μ. Peak transconductance is relatively constant with changing channel length, whereas the low-field mobility shows a decreasing trend with channel length. The dashed lines are guide to the eye.***

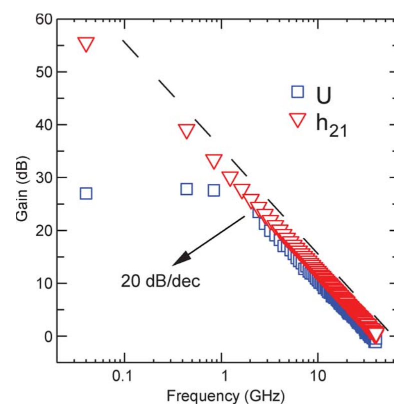


Fig. 9. ***Current gain (h_{21}) and unilateral power gain (U) after de-embedding. The f_T is 44 GHz and the $f_{\max} = 34$ GHz for this 600-nm channel-length device [41]. The dashed line follows the slope of 20 dB/decade.***

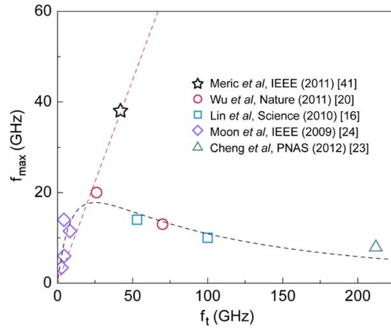
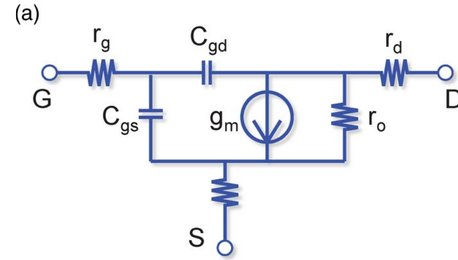


Fig. 10. $f_{\max}$ ***versus*** f_T ***for graphene devices reported in literature. Star indicates measurement from an hBN-supported device. All other symbols correspond to devices fabricated with conventional oxide dielectrics. Dashed black curve represents a guide to the eye for the data from oxide-based devices. Red dashed line indicates the expected scaling behavior for the hBN-supported device [41].***

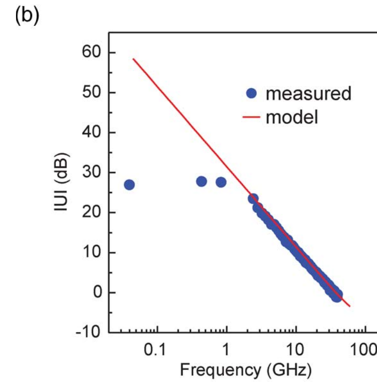
achievable $f_{\max}$ already outperforms oxide-dielectric-based devices that have up to ten times shorter gate lengths. We note that the $f_{\max}/f_T$ ratio for this device is as high as 0.86, significantly greater than the value typically observed for GFETs fabricated with oxide-based dielectrics. Fig. 10 compares the f_T and $f_{\max}$ of representative devices from the literature. The ratio of the two values is close to one for hBN devices, while for the oxide-supported GFETs the $f_{\max}/f_T$ ratio is consistently less than 0.4. If current saturation can be maintained with channel-length scaling for hBN-supported devices, $f_{\max}$ values of up to 300 GHz could be achievable at 100-nm channel length [41].

We use the small-signal-equivalent circuit in Fig. 11(a) to model the high-frequency response of the GFETs. Good agreement is obtained with the measured unilateral gain, as shown in Fig. 11(b), using the component values in Fig. 11(c). The extracted small-signal values are also in good agreement with values derived from the I–V characteristics. From these extracted values, we can also identify three significant limitations on high-frequency performance for existing GFET technologies. First, the bias point for this characterization is chosen to maximize transconductance. Because we do not have independent control of the CNP in these devices, however, this does not correspond to the bias of maximum output resistance. The value of the output resistance r_o could be increased from 100 to nearly 500 Ω through independent CNP control. Second, a significant portion of the channel capacitance is apportioned to the drain with $C_{gd}/C_{gs} = 0.5$, significantly higher than in silicon devices. This is expected to improve with better current saturation. Finally, achieving good contacts to graphene remains problematic, as described in Section II. From the small-signal model, the contact resistance is estimated to be 950 $\Omega\mu$m. While typical for GFETs reported in the literature, this contact resistance is more than two orders of magnitude larger than in traditional silicon devices. The $f_{\max}$ of the device in Fig. 11 would be

(a)



(b)



(c)

g_m	19 ms	r_s, r_d	12.5 Ω
r_o	98 Ω	C_{gd}	17 fF
r_g	19 Ω	C_{gs}	34 fF

Fig. 11. ***Small-signal modeling. (a) The small-signal-equivalent circuit used to model the high-frequency behavior of GFETs. (b) Unilateral power gain of both measured and modeled devices. (c) Small-signal values used in the model to obtain the fit in (b).***

improved by a factor of two if the contact resistance could be reduced to 40 $\Omega\mu$m, which is the theoretical minimum value [45].

IV. BANDGAP

While exploiting graphene for RF applications does not require the existence of a bandgap *per se*, theoretical calculations indicate that inducing even a modest gap, on the order of only 100 meV, would optimize small-signal circuit performance [46]. Furthermore, a small gap could significantly improve device performance in short-channel devices by limiting band-to-band tunneling processes. This holds practical relevance since opening a bandgap in graphene is possible by several techniques.

By etching graphene into narrow "ribbons," a bandgap can be induced by lateral confinement, where the gap varies inversely with the width of the ribbon. Gaps as large as 200 meV have been achieved in graphene nanoribbons [47], and, in principle, gaps larger than 0.5 eV can be achieved for device widths less than 5 nm [48]. Fabrication of such devices remains a difficult technological challenge, particularly on the wafer scale. More problematic, carving graphene into nanoribbons by plasma etching leaves the

device edges highly disordered. In the case of ultranarrow ribbons, this edge disorder dominates transport characteristics, and mobility decreases dramatically, offsetting the potential benefits graphene may offer over silicon [49].

More generally, any process that lifts the degeneracy of the A–B sublattice will open a gap in the energy spectrum. Uniaxial strain has been proposed as one way to achieve this; however, the expected strain required to open a gap is in excess of 20%, which is technologically infeasible [50]. Alternatively, several calculations have suggested that if graphene could be epitaxially aligned to hBN, the difference in interaction energy between the carbon–boron and carbon–nitrogen atoms would open a gap as large as 50 meV [7]. To date, no experiments have been successful at controlling the crystallographic alignment in hBN-supported graphene structures, and in the several studies of graphene on hBN, no one has yet reported evidence of such a bandgap [31].

Bilayer graphene, consisting of two Bernal-stacked graphene sheets, also exhibits a gapless bandstructure intrinsically. However, application of a transverse electric displacement field breaks the layer symmetry, resulting in a gap proportional to the applied field [51]. This *gate-tunable bandgap* is a unique feature of bilayer graphene and has generated significant technological interest, especially in the area of tunable optoelectronics. For high-frequency FET devices, the ability to induce a bandgap offers the possibility of enhancing saturation characteristics and thereby overcoming the low output resistance that so far limits $f_{\max}$ in short devices. Recent high-bias measurements in a dual-gated bilayer FET indeed demonstrate enhanced voltage gain by up to a factor of six larger than similar monolayer devices [52]. In order to utilize bilayer graphene for RF applications, two outstanding issues will need to be addressed. First, bilayer devices fabricated on SiO_2 typically exhibit much lower mobility than in single layers [53]. Second, while a field effect gap as large as 200 meV has been verified optically, the corresponding transport gap is substantially reduced by disorder in electrical transport [54]. The use of hBN dielectrics as both top and bottom gate dielectrics may substantially overcome both of these issues [55]. Early experiments indicate that bilayer graphene fabricated on hBN dielectrics show superior transport characteristics in comparison to similarly fabricated monolayer devices [31]. Furthermore, encapsulated monolayer graphene devices with hBN forming both the top and bottom dielectrics (using the same fabrication techniques as outlined in Fig. 4) are found to show optimal transport in both the low-bias and high-bias regimes [35], [42], [56]. Provided that a similar hBN-encapsulated GFET structure would allow for comparable enhancements in the electronic properties of bilayer graphene (as have been observed for monolayer samples), a transport gap could be observable in bilayer GFETs, even at room temperature. So far, no studies have reported high-frequency characteristics of *gapped* monolayer or bilayer graphene devices. This represents an important outstanding experiment that may enable a crucial step forward in graphene-based technologies, particularly when combined with further channel length scaling.

V. WAFER-SCALE FABRICATION

A fundamental requirement for commercial electronic applications will be to develop wafer-scale processes for manufacturing both high-quality graphene and hBN. Growth of large-area films by chemical vapor deposition (CVD) grown on low-cost substrates promises a method to produce graphene suitable for commercial applications. Graphene growth has already made important advancements in the last few years [58], [59]. For example, it is now possible to grow single-crystalline graphene samples up to a few hundred micrometers in size [60], using optimized CVD growth techniques. By combining this large-grain growth with hBN dielectrics, it was recently shown that CVD-grown devices can exhibit transport quality comparable to those of graphene exfoliated from natural graphite [57], [61]. Fig. 12 shows the four-probe resistivity and field-effect mobility of such a sample with hBN dielectric. Remarkably, the field-effect mobility is close to 30 000 cm^2/Vs at the highest density [57].

As the interest in hBN as a dielectric for graphene is rather new, limited large-scale growth capabilities for hBN films have been developed. However, there are recent attempts to grow controlled thickness of hBN [62]–[65], to directly grow graphene on hBN [66], and to grow

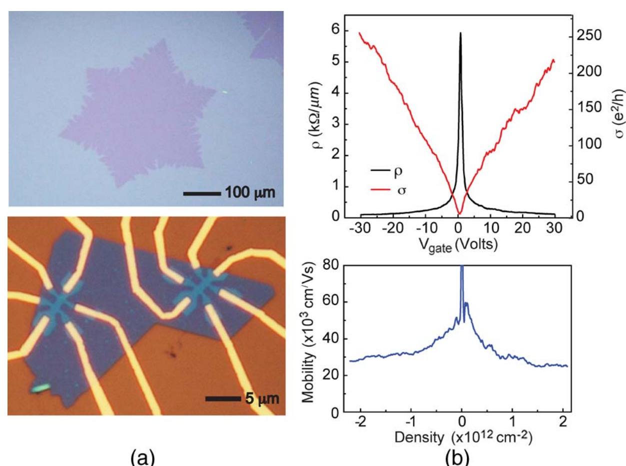


Fig. 12. *CVD graphene on hBN [57]. (a) Upper panel shows an optical image of a large single-crystalline graphene flake grown by low-pressure CVD. Lower panel shows a Hall bar device fabricated after transferring the graphene to an hBN substrate. (b) Low-field transport measurements taken from the Hall-bar geometry shown in (a) ($T = 1.5$ Kelvin). Lower panel shows the field-effect mobility plotted as a function of carrier density. A high-density mobility of 30 000 cm^2/Vs is measured, which is comparable to the best exfoliated devices on hBN, at equivalent carrier density.*

alternating layers of graphene/hBN [67]. While these attempts are in their infancy and devices are currently of low quality, these techniques promise to soon enable fully scalable growth of graphene/hBN heterostructures for a wide range of applications [68].

VI. CONCLUSION

In this review, we summarize the recent progress in using hBN as a dielectric for graphene FETs. The use of hBN significantly reduces impurities and charged traps associated with the gate dielectric and graphene/dielectric interface over metal–oxide alternatives. Additionally, fabrication of layered graphene/hBN heterostrucutres is accomplished without the need for an adhesion layer, allowing the intrinsic properties of the graphene channel to be maintained. I–V characteristics from hBN-supported devices show saturating drain current behavior down to the shortest channel lengths currently measured (0.5 μm) and to date yield the record peak dc voltage gain. RF measurements of these devices show significantly improved $f_{\max}$ and, more importantly, $f_{\max}/f_T$ ratios. If continued channel-length scaling into the sub-100-nm region with saturating I–V characteristics can be achieved and device parasitics can be further controlled, $f_{\max}$ values approaching the terahertz regime may be expected. Further process development is necessary to realize wafer-scale growth of graphene/hBN heterostructures and enable fabrication of high-performance GFETs on a large scale. ■

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