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Graphene Field-Effect Transistors for Radio-Frequency Flexible Electronics

NICHOLAS PETRONE[1], INANC MERIC[1,2], TARUN CHARI[3], KENNETH L. SHEPARD[3] (Fellow, IEEE), AND JAMES HONE[1]

[1]Mechanical Engineering Department, Columbia University, New York, NY 10023 USA
[2]Intel Corporation, Hillsboro, OR 97124 USA
[3]Electrical Engineering Department, Columbia University, New York, NY 10023 USA

CORRESPONDING AUTHOR: N. PETRONE (e-mail: nwp2105@columbia.edu)

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ABSTRACT Flexible radio-frequency (RF) electronics require materials which possess both exceptional electronic properties and high-strain limits. While flexible graphene field-effect transistors (GFETs) have demonstrated significantly higher strain limits than FETs fabricated from thin films of Si and III-V semiconductors, to date RF performance has been comparatively worse, limited to the low GHz frequency range. However, flexible GFETs have only been fabricated with modestly scaled channel lengths. In this paper, we fabricate GFETs on flexible substrates with short channel lengths of 260 nm. These devices demonstrate extrinsic unity-power-gain frequencies, f_{max}, up to 7.6 GHz and strain limits of 2%, representing strain limits an order of magnitude higher than the flexible technology with next highest reported f_{max}.

INDEX TERMS Chemical vapor deposition (CVD), FET, flexible electronics, grapheme, radio-frequency (RF).

I. INTRODUCTION

The desire to integrate wireless communications into flexible electronics requires field-effect transistors (FETs) which both demonstrate unity-power-gain cut-off frequencies, f_{max}, in the gigahertz frequency range and can withstand high levels of strain. While the highest electronic performance for flexible radio-frequency FETs (RF-FETs) have been achieved in thin films of Si and III-V semiconductors laminated on polymer substrates, poor mechanical flexibility has restricted strain limits in these devices typically to below ~0.25% [1], [2], with pre-straining resulting in slightly improved strain limits in tension up to 1.08% [3].

In contrast, graphene is an ideal candidate for use in flexible RF-FETs, because it offers both exceptional electronic properties (room temperature mobility in excess of 10,000 $cm^2\ V^{-1}\ s^{-1}$ and saturation velocity of 1-5 $x10^7$ cm s^{-1}), as well as outstanding mechanical performance (strain limits up to 25%) [4], [5]. Furthermore, large-area films of graphene can be produced in commercially scalable processes by chemical vapor deposition (CVD) [6], which demonstrate equivalent electronic and mechanical properties to pristine graphene crystals [7], [8]. Indeed, flexible RF-FETs have been fabricated from CVD graphene which demonstrated f_{max} up to 3.7 GHz with strain limits up to 1.75% [9]. Strain limits up to 8% have been achieved in flexible GFETs with f_{max} = 2.1 GHz [10].

While graphene RF-FETs have demonstrated improved mechanical performance over those fabricated from Si and III-V semiconductors, electronic performance has remained in the low gigahertz frequency range. However, flexible graphene RF-FETs have only been fabricated with modestly scaled channel lengths down to 500 nm [9], [10], allowing for the potential to improve f_{max} to a level competitive with traditional semiconductors by channel length scaling [4]. In this work, we fabricate flexible RF-FETs with CVD graphene as the active channel material with a 260-nm channel length. The devices demonstrate extrinsic f_{max} up to 7.6 GHz, with strain limits up to 2%. This work not only

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achieves the highest extrinsic RF performance reported for flexible GFETs to date, but also demonstrates a strain limit an order of magnitude higher than in thin films of InAs, the flexible RF-FET technology with best competing f_{max} [2].

II. DEVICE FABRICATION

Graphene field-effect transistors (GFETs) were fabricated on flexible and transparent polyethylene naphthalate (PEN) substrates. Novel fabrication procedures enabled the production of flexible GFETs at 260 nm. PEN was mounted on a rigid substrate for device fabrication and an optimized device structure was utilized, enabling enhanced electron-beam lithography (EBL) resolution and alignment precision; indeed, this work presents the shortest channel GFETs fabricated from CVD graphene on a flexible substrate to date [9], [10].

PEN substrates were first adhered to Si handle substrates using a thin film (~6 μm) of polydimethylsiloxane (PDMS) as an adhesive layer. Dual-fingered bottom gates were patterned on the PEN substrates by EBL followed by evaporation of 1 nm Cr/20 nm Au-Pd alloy (60-40 wt. %) and lift-off. Next, a 6-nm gate dielectric of HfO_2 ($\kappa \approx 13$) was grown by atomic layer deposition (ALD). CVD graphene was synthesized and subsequently transferred over the gate utilizing procedures previous described in literature [7]. The graphene channel was defined by EBL and etched in an oxygen plasma. GFET fabrication was finished by contacting the channel with source and drain electrodes (1 nm Cr/20 nm Pd/110 nm Au) which overlap the gate. Devices were fabricated with a total gate length of 400 nm: source-gate and drain-gate overlap were ~70 nm, resulting in a gated channel length of 260 nm (equivalent to the source-drain spacing). The dual-fingered device has a total channel width of 20 μm. For purposes of de-embedding high frequency data, standard 'open' and 'short' test devices were simultaneous fabricated on-chip with dimensions equivalent to GFETs. Dimensions of the RF-FET and de-embedding structures were verified by scanning electron microscope (SEM) imaging, ensuring fidelity of fabrication and accuracy of de-embedding methods.

Fig. 1 shows an array of RF-FETs and de-embedding structures on PEN both prior to (a) and after (b) mechanical release from the Si handle substrate. A false-colored SEM image and a cross-sectional schematic of a flexible RF-FET are shown in Fig. 1(c) and (d).

III. RESULTS AND DISCUSSION

Fig. 2(a) shows device resistance, R, plotted as a function of gate-to-source voltage, V_{gs}, measured at a fixed source-to-drain bias, V_{sd} = 10 mV. For the device presented in Fig. 2(a), the low-field field-effect mobility was $\mu_{FE} \approx 1000$ cm^{2}V^{-1}s^{-1}, calculated as $\mu_{FE} = (L_{ch}g_m)/(W_{ch}C_{tot}V_{sd})$, where g_m is the measured small-signal transconductance, L_{ch} is the gated channel length (260 nm), W_{ch} is the effective channel width (20 μm), and C_{tot} is the total effective gate capacitance per unit area

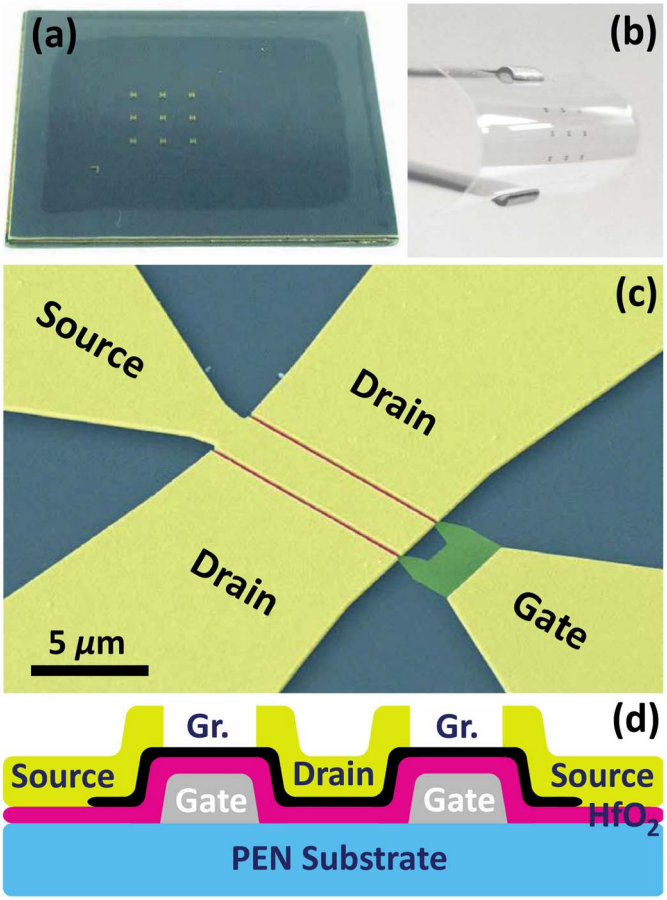

FIGURE 1. (a) and (b) Photograph of graphene FET (GFETs). De-embedding structures fabricated on a flexible and transparent PEN substrate both (a) mounted on and (b) released from a Si-handle substrate. (c) False-colored scanning electron micrograph and (d) cross-sectional schematic of a flexible GFET. Channel length is 260 nm and effective channel width is 20 μm.

(920 nF cm^{-2}), computed as the series combination of the electrostatic capacitance ($C_e \approx 1700$ nF cm^{-2}) and the quantum capacitance ($C_q \approx 2000$ nF cm^{-2} for the pertinent carrier density range) [11].

Fig. 2(b) plots high-bias current-voltage (I–V) characteristics of the flexible GFET, for which the measured drain current, I_d, is plotted as a function of V_{sd} at fixed values of V_{gs} decreasing from 0 V to -1.5. High-field values of g_m and output resistance, r_o, are extracted from the I–V characteristics and are plotted as a function of V_{gs} and V_{sd} in Fig. 2(c) and (d). Maximum g_m = 7.6 mS (0.38 mS/μm) is achieved at a bias point of V_{sd} = 0.5 V and V_{gs} = −0.5 V. At this bias point, r_o = 123 Ω, only slightly less than a maximum of 157 Ω obtained at V_{sd} = 0.33 V, V_{gs} = 0 V. While values of g_m and r_o are less than the highest reported values for GFETs on solid substrates [4], they are comparable to values reported for GFETs on flexible substrates [9], [10].

Fig. 3(a) plots current gain (h_{21}) and unilateral power gain (U) as a function of frequency for the flexible GFET. Both h_{21} and U are extracted from S-parameters measured at the bias point that maximizes

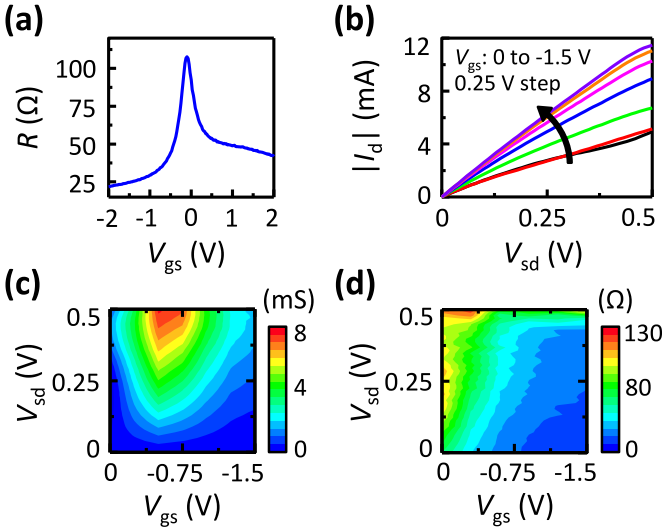

FIGURE 2. **DC characteristics of flexible graphene FET. (a) Device resistance, *R*, plotted as a function of gate-to-source voltage; V_{gs}, at a source-to-drain bias; and V_{sd}, of 10 mV. (b) Transfer (*I–V*) characteristics which plot drain current, I_d, against V_{sd}. *I–V* curves are taken at fixed V_{gs} decreasing from 0 V (black) to -1.5 V (purple) in increments of 0.25 V. (c) Transconductance, g_m. (d) Output resistance, r_o, plotted as a function of V_{sd} and V_{gs}.**

g_m (V_{sd} = 0.5 V, V_{gs} = -0.5V, see Fig. 2(c)). At this bias point, the device is operated as a unipolar p-type channel. The as-fabricated device demonstrates a cut-off frequency for unity current gain, f_T, and f_{max} of 23.6 GHz and 6.5 GHz, respectively. These values represent ~2x improvement in f_T and f_{max} over the previous highest values report in flexible GFETs fabricated at a channel length of 500 nm [9]. The cut-off frequency in terms of unity maximum available gain (MAG) is 6.6 GHz.

Conservative open and short de-embedding methods ('pad de-embedding') were employed implementing an open structure that includes only the parasitic capacitance of the electrode pads and has a source-drain spacing of 600 nm (no overlap of source and drain electrodes with the gate). Fig. 3(b) plots h_{21} and U as a function of frequency after performing pad de-embedding. Extrinsic f_T and f_{max} are found to be 38.7 GHz and 7.6 GHz, respectively. These are the first flexible GFETs to demonstrate extrinsic power gain at all frequencies up to 7.6 GHz, a technologically pertinent frequency range currently used for most wireless communication.

To better analyze the accuracy of the pad de-embedding methods employed in this work, gate capacitance, C_g, was extracted from measured scattering parameters and compared with the expected value for C_{tot} of 920 nF cm^{-2}. Prior to de-embedding C_g = 1250 nF cm^{-2}, indicating that parasitic capacitances related to the electrode pads comprise ~330 nF cm^{-2}of the total device capacitance and constitute a dominant limitation to RF performance. However, after performing pad de-embedding C_g is extracted as 885 nF cm^{-2}, in excellent agreement with the value expected for the GFET channel geometry. Pad de-embedding is thus seen

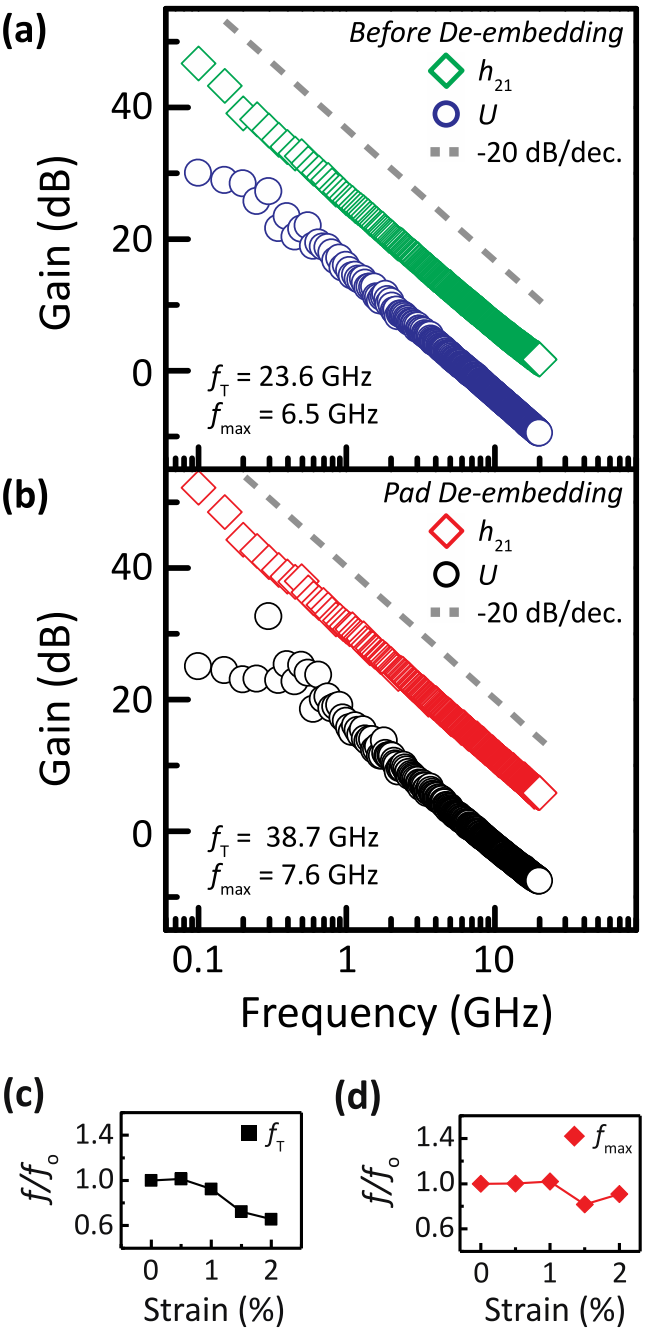

FIGURE 3. **RF characteristics of graphene FET. Current gain, h_{21}, and unilateral power gain, *U*, plotted as a function of operation frequency on both (a) prior to and (b) after pad de-embedding. Values of f_T and f_{max} are presented. Dashed line in both plots indicates a -20 dB/dec. slope, included to demonstrate that this frequency dependence is followed both prior to and after de-embedding. (c) f_T and (d) f_{max} normalized by their unstrained values are plotted as a function of strain.**

to accurately remove parasitic capacitances resulting from the electrode pads of the fabricated GFETs and thus functions to provide a reliable estimate for the extrinsic RF performance of the GFET itself. We note that while 'full de-embedding' procedures (which employ an open structure with dimensions equivalent to the FET being measured) are more commonly employed in measurement of graphene

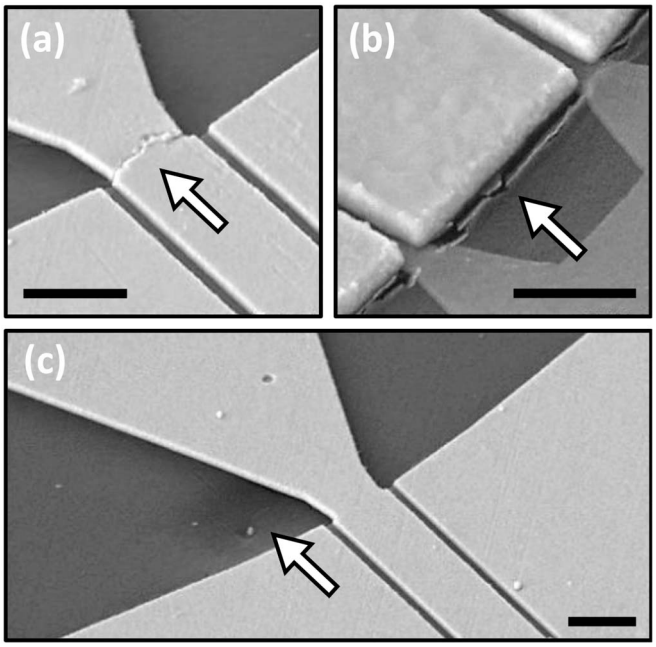

FIGURE 4. Scanning electron micrograph of GFET after (a) mechanical and (b) and (c) thermal failure. (a) Cracks develop in the source electrode at strains greater than 2%. Joule heating in the device causes (b) warping of the substrate and overlaying GFET. (c) Cracking of the HfO_2 dielectric. Scale bars are 2 μm in panels (a) and (c) and 1 μm in panel (b).

field-effect transistors, this process removes parasitics related to all metal interconnects, even those required by a device integrated in a functional circuit, and thus results in calculated cut-off frequencies that are practically unattainable [12] (see Appendix for further details).

The increase in f_T and f_{max} from previously reported flexible GFETs fabricated at 500 nm can be attributed to channel length scaling in conjunction with improvements to device architecture. Previous works utilize a device structure with un-gated spacer regions in the graphene channel that increase total contact resistance and degrade RF performance [9], [10]. In this work by overlapping the source/drain electrodes with the gate, these resistive spacer regions are eliminated to effectively reduce contact resistance (less than 200 Ω-μm). Trends in devices fabricated on rigid substrates indicate that the RF performance of flexible GFETs will likely benefit from further channel length scaling [13], [14]. Additionally, these devices demonstrate increased intrinsic voltage gain ($g_m r_o$ = 0.93) at the bias point at which RF characterization is performed [9]. $g_m r_o$ is largely limited by the inability to bias the current devices strongly into saturation because of thermal limitation.

Mechanical limits of flexible RF-FETs were subsequently determined by measuring electronic characteristics while simultaneously applying uniaxial tensile strain, ε, orthogonal to the device channel under two-point bending [9]. Fig. 3(c) and (d) demonstrate that f_T and f_{max} exhibit less than 35% and 20% degradation, respectively, from their unstrained values over the entire measured strain range (ε = 0-2%). No significant variation in source-to-gate current was observed up to 2% strain, indicating negligible leakage through the dielectric.

Devices were strained to the point of mechanical failure. Fig. 4(a) shows that at strains greater than 2%, cracks form in the source/drain electrodes, corresponding to irreversible degradations in electronic characteristics (measurement of open-circuit voltage). Because the strain limit of the device is limited by the electrodes rather than by the graphene channel, improved flexibility potentially is achievable by implementing electrode materials with higher strain limits, such as graphite.

It is significant to note that the RF performance of the device is limited by thermal constraints of the substrate. At V_{sd} greater than ~0.5 V, Joule heating in the device channel results in local melting of the PEN substrate, irreversible warping of the GFET channel, and cracking of the HfO_2 dielectric as shown in Fig. 4(b) and (c). Limitations to the range of electric field that can be applied prevent devices from reaching full current saturation, limiting the achievable $g_m r_o$ and cut-off frequencies. Improvements to thermal management which allow for higher current densities, such as utilizing substrates with higher glass transition temperatures [10], will allow the devices to be biased into saturation, improving r_o and device intrinsic voltage gain.

IV. CONCLUSION

We present flexible RF-FETs fabricated from CVD graphene with 260 nm channel lengths that demonstrate extrinsic f_{max} up to 7.6 GHz and ultimate strain limits of 2%. These values not only represent the highest reported extrinsic f_{max} in any flexible GFET technology to date, but they also show an order of magnitude improvement in strain limit over the flexible technology demonstrating the best competing RF performance. This work further establishes the potential of CVD graphene to enable electronics that demonstrate both high frequency operation and high mechanical flexibility. Future improvements to thermal management are essential to further improve the RF performance of flexible GFETs.

APPENDIX

'Full de-embedding' uses the intrinsic transistor as an open structure. It is identical in dimension and design to the transistor but does not include the graphene channel material. However, full de-embedding results in the de-embedding of not only the electrode pads but the metal interconnects (and their associated capacitances) in the device structure. While the intent of this de-embedding approach is to determine the intrinsic performance of the active FET channel, in practice full de-embedding over-compensates by removing parasitics related to components of the device required for integration into a practical circuit. The result is an inflated estimate of the cut-off frequencies beyond what is achievable in a practical FET fabricated at equivalent channel lengths. Unfortunately, this de-embedding is the most commonly used de-embedding structure for experimental GFET technologies [12].

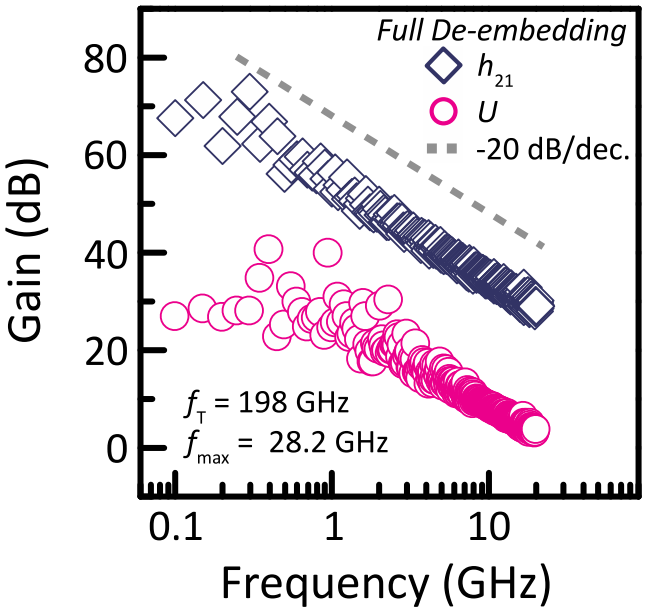

FIGURE 5. RF characteristics of a flexible, graphene FET after performing full de-embedding. Current gain, h_{21}, and unilateral power gain, U, are plotted as a function of operation frequency. Intrinisc f_T and f_{max} are presented. Dashed line indicates a -20 dB/dec. slope.

For demonstrative purposes, we perform full de-embedding on our flexible devices utilizing an open de-embedding structure equivalent to that of the GFET under test. Fig. 5 plots h_{21} and U as a function of frequency after performing full de-embedding. Intrinsic f_T and f_{max} are found to be 198 GHz and 28.2 GHz respectively. Full de-embedding results in a value of f_T that is a full order of magnitude higher than the value prior to de-embedding. Indeed, full de-embedding results in C_g = 92 nF cm^{-2} (as extracted from measured scattering parameters), similarly a full order of magnitude below the value expected for the channel geometry alone (920 nF cm^{-2}). These findings warn of the importance of implementing accurate de-embedding methods during RF characterization.

Although cut-off frequencies extracted from full de-embedding cannot be take as an accurate measurement of the intrinsic device performance, they do allow for direct comparison of RF performance with previously reported flexible FET technologies implementing equivalent de-embedding procedures [2], [3], [10], [13], [14]. Indeed, f_T of 198 GHz measured in this work is significantly higher than the best value previously reported for flexible GFETs (intrinsic $f_T \sim 25$ GHz for 500 nm channel length) [10], and comparable to GFETs fabricated on rigid substrates at similar channel lengths [13]. f_{max} of 28.2 GHz is not only an order of magnitude higher than previously reported for flexible GFETs fabricated at channel length of 500 nm [9], [10] but also the highest intrinsic f_{max} reported in any flexible technology to date [1]–[3]. Furthermore, these devices exhibit an order of magnitude improvement in strain limit over the flexible technology demonstrating the next highest intrinsic f_{max} [2].

While a comparison of intrinsic cut-off frequencies extracted after full de-embedding does not permit an accurate quantitative assessment of device performances, it does enable a qualitative demonstration of the improved electronic performance of the graphene channel in this work.

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Authors' photographs and biographies not available at the time of publication.