Properties of Self-Aligned Short-Channel Graphene Field-Effect Transistors Based on Boron-Nitride-Dielectric Encapsulation and Edge Contacts

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***Abstract*— We present the characterization of ballistic graphene field-effect transistors (GFETs) with an effective oxide thickness of 3.5 nm. Graphene channels are fully encapsulated within hexagonal boron nitride, and self-aligned contacts are formed to the edge of the single-layer graphene. Devices of channel lengths (L_G) down to 67 nm are fabricated, and a virtual-source transport model is used to model the resulting current–voltage characteristics. The mobility and source-injection velocity as a function of L_G yields a mean-free-path, ballistic velocity, and effective mobility of 850 nm, 9.3×10^7 cm/s, and 13 700 cm^2/Vs, respectively, which are among the highest velocities and mobilities reported for GFETs. Despite these best-in-class attributes, these devices achieve transconductance (g_m) and output conductance (g_{ds}) of only 600 and 300 μS/μm, respectively, due to the fundamental limitations of graphene's quantum capacitance and zero-bandgap. g_m values, which are less than those of comparable ballistic silicon devices, benefit from the high ballistic velocity in graphene but are degraded by an effective gate capacitance reduced by the quantum capacitance. The g_{ds} values, which limit the effective power gain achievable in these devices, are significantly worse than comparable silicon devices due to the properties of the zero-bandgap graphene channel.**

***Index Terms*— Graphene field-effect transistor (GFET), heterostructures, quantum capacitance, virtual source (VS).**

I. Introduction

GRAPHENE, the single-atom thick, hexagonally latticed carbon allotrope, has drawn significant interest as an electronic channel material for field-effect transistors (FETs) on both rigid [1]–[4] and flexible substrates [5]–[8] due to its high low-field carrier mobility (>1 000 000 cm^2/Vs at room temperature [9], [10]), atomically thin form, and exceptional mechanical flexibility (1-TPa Young's modulus [11]). Graphene, however, does not possess a bandgap, creating the possibility for ambipolar conduction in the channel under appropriate bias conditions. The lack of a bandgap also makes it difficult to turn the device OFF, resulting in low peak ON-current-to-OFF-current ratios (at best, less than 100 [12]) and making these devices largely impractical for digital applications. Instead, efforts have been focused on exploiting graphene FETs (GFETs) for analog and RF applications which require power amplification and take the advantage of device transconductance (g_m) and output conductance (g_{ds}). A number of alternate 2-D materials for devices have been proposed, including materials that have a bandgap, such as MoS_2 [13]; bilayer devices, including graphene bilayer devices [14]; and heterostructure devices that include graphene combined with wider bandgap materials [15]. None of these alternate materials has yet achieved the mobilities of boron nitride (BN)-encapsulated single-layer graphene.

GFET devices have traditionally been challenged by poor dielectric interfaces and poor ohmic contacts. Graphene's electrical transport properties are strongly affected by anything in contact with its surface; among the highest reported mobilities are those of graphene suspended in vacuum [10]. Carrier mobilities and transport velocities are negatively impacted by impurities adsorbed on exposed graphene surfaces by charge-trapping states at graphene–dielectric interfaces. GFETs have typically been fabricated on silicon dioxide substrates with a top-gate dielectric thickness greater than 5 nm, made from high-κ materials, such as HfO_2 or Al_2O_3 [grown by atomic layer deposition (ALD)]. These devices exhibit low-field mobilities that are typically less than 1000–3000 cm^2/Vs [1], [16], [17] and significant hysteresis with changes in gate voltage due to trapped charge from the substrate and gate oxide [18], [19]. Contacts are conventionally formed by depositing metal over an area of the graphene surface to form the source and drain. These approaches yield a contact resistance that is typically 1 kΩ-μm and no better than 200 Ω-μm [20]–[23]. Device current–voltage (I–V) characteristics for GFETs, particularly at short-channel lengths (L_G), have generally not shown strong saturating characteristics, due in part to these large contact resistances combined with the relatively poor electrostatics of the large oxide thickness (t_{ox}).

The use of hexagonal BN (h-BN) for dielectric encapsulation of graphene allows low-field mobilities in excess

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of 1 000 000 cm^2/Vs to be achieved at room temperature in these heterostructures [9], comparable with the best mobilities achieved in suspended samples [10]. Like graphene, h-BN is a hexagonally latticed crystal, exhibiting strong in-plane bonding. Consequently, there are no out-of-plane dangling bonds, making it an ideal substrate and gate dielectric for graphene [24]. Furthermore, its layered structure permits the use of extremely thin h-BN to serve as the gate dielectric, permitting small effective oxide thickness (EOT). Though attempts have been made to use a graphene/h-BN heterostructure as an FET, the graphene in these structures has still been exposed to impurities during fabrication, leading to less than optimal device characteristics [25], [26].

In this paper, we present the first short-channel self-aligned GFETs (<100 nm) based on full h-BN encapsulation of the graphene sample [9]. Source and drain contacts are formed by making edge contact to the graphene; this is also the first time that this contact technology has been used in a short-channel FET structures. Electrical contact to the edge of graphene yields remarkably low contact resistances, 100 and 200 Ω-μm for electrons and holes, respectively, close to the minimum possible as determined by Landauer–Buttiker considerations. There have been reports of areal contacts achieving comparable or slightly better contact resistivity on epitaxial graphene on SiC substrates [27], but the quality of epitaxial graphene is generally lower than that achieved with graphene grown by other means (such as chemical vapor deposition on copper) or mechanically exfoliated from bulk crystal. This asymmetry in contact resistance is opposite to that observed for conventional top contacts, where the contact resistance for holes is generally lower than that for electrons. Consequently, most GFETs are biased as p-type devices, while the devices presented here are biased as n-type transistors.

II. Fabrication

To assemble the encapsulated h-BN/graphene/h-BN heterostructures, a van der Waals mechanical transfer technique is employed [9]. First, graphene and h-BN crystals are exfoliated on 285-nm SiO_2 on Si substrates. The h-BN is characterized by atomic force microscopy (AFM) to verify the thickness of the crystals. Next, a thin h-BN is selected to serve as the gate dielectric and then lifted from the SiO_2 surface using a polymer handle. This h-BN crystal is then used to pickup the monolayer graphene, which is then transferred onto a relatively thicker (>15 nm) h-BN crystal that serves as the device substrate. The assembled heterostructure is vacuum annealed at 350 °C for 15 min at $<2 \times 10^{-7}$ mbar to remove polymer residue left during the transfer process [Fig. 1(a)]. Characterization by AFM yields a pristine, bubble-free heterostructure.

In most GFET structures, an additional ungated, intrinsic graphene region is present; this is a source of substantial additional contact resistance. In our case, edge contacts are combined using a self-aligned process that effectively eliminates these spacer regions. Starting from the encapsulated graphene heterostructure, transistor fabrication proceeds, as shown in Fig. 1. We use e-beam lithography to define the local top gates using a bilayer resist consisting

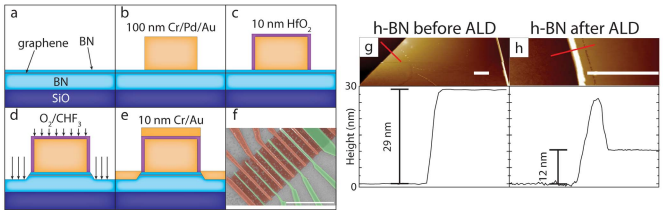

Fig. 1. Summary of fabrication. (a) Assembly of h-BN/graphene heterostructure. Black line separating the blue areas: monolayer graphene. Blue areas: h-BN. (b) Deposition of local top gate >100-nm Cr/Pd/Au. (c) ALD of 10-nm HfO_2. (d) CHF_3/O_2 plasma etch to expose the graphene edge. (e) 10-nm Cr/Au deposition for self-aligned source–drain contacts. (f) False color: SEM image of several GFETs. Red areas: source–drain contacts and leads. Green areas: local gates. (g) AFM image of a single, freshly exfoliated h-BN crystal on a SiO_2 substrate. Line cut reveals that it is 29-nm thick. (h) AFM image of the same h-BN crystal in (g) after HfO_2 growth. Line cut reveals that h-BN thickness is now 12 nm, a difference of 17 nm, due to the HfO_2 growing on the SiO_2 substrate but not on the interior surface of the h-BN crystal. Scale bar is 2 μm.

of 200 nm of a copolymer below 100 nm of poly (methyl methacrylate) (PMMA). The gate metal stack is 2 nm of Cr, 20 nm of Pd, and 100 nm of Au [Fig. 1(b)]. Following the deposition of the gate metal, we anneal the device at 350 °C for 15 min at $<2 \times 10^{-7}$ mbar vacuum to remove any PMMA residue (as measured by AFM). Next, we deposit 10 nm of HfO_2 by ALD to electrically isolate the gate [Fig. 1(c)]. Because h-BN is atomically smooth, it is resistant to the nucleation of HfO_2; HfO_2, therefore, grows everywhere except on the surface of h-BN.

This selective growth of HfO_2 is highlighted in Fig. 1(g) and (h), in which an exfoliated 29-nm-thick h-BN crystal on SiO_2 is shown before and after the growth of 15 nm of HfO_2 by ALD. The step height change of 17 nm between the two images indicates that the HfO_2 has been deposited on the SiO_2 and the edge of the h-BN but not on the interior of the crystal.

Following the HfO_2 deposition, we plasma etch the heterostructure (4-sccm O_2 and 40-sccm CHF_3 plasma under 60-W dc power for 15 s) to expose the edge of the graphene [Fig. 1(d)]. E-beam lithography is then used to define the source–drain contacts. Then, we evaporate 1.5-/10-nm Cr/Au to make electrical contact with the graphene edge [Fig. 1(e)]. Finally, the thick (100 nm) gold leads and probe pads are evaporated to provide low resistance connections to the devices. Fig. 1(f) shows a false color image of the device structure with green representing the local gates and red representing the source–drain contacts.

III. Electrical Characterization and Modeling

The I–V characteristics of five encapsulated GFETs with L_G of 67, 103, 122, 178, and 1240 nm, as determined by scanning electron microscopy (SEM), are measured [Fig. 2(a)]. These devices are all fabricated from the same heterostructure, sharing the same 3.5-nm-thick top h-BN crystal as the gate dielectric (EOT of ∼3.5 nm [28] given a dielectric constant for h-BN which closely matches that of silicon dioxide). The oxide capacitance (C_{ox}), therefore, is estimated to be 10 fF/μm^2, about three times less than the C_{ox} for silicon devices at the 65-nm technology. The choice of h-BN

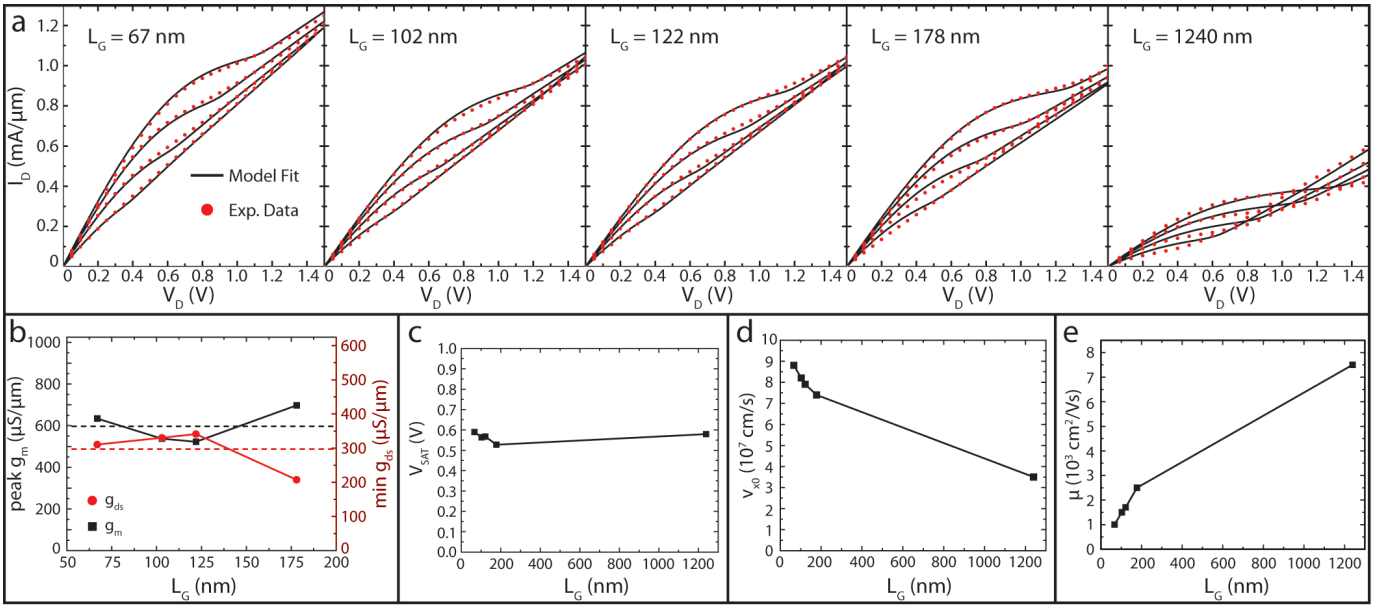

Fig. 2. (a) Output characteristic of GFETs of varying L_G values. Gate voltage increases from 0.5 to 1.1 V. Dotted curves: experimental data. Solid curves: VS model fits. (b) Sub-200-nm channel length devices exhibit similar output characteristics with g_m of 600 μS/μm and g_{ds} of 300 μS/μm. Dotted lines: average values of g_m and g_{ds} for the sub-200-nm channel length devices. (c)–(e) V_{SAT}, v_{x0}, and μ extracted from the VS model with L_G. V_{SAT} is found to be constant at ~0.55 V, v_{x0} with decreasing L_G, and μ decreasing with decreasing L_G.

thickness is based on the limitations of fabrication. Building this heterostructure using <5-nm-thick top h-BN crystals is extremely challenging because the crystal tends to develop physical defects (such as cracks) during the transfer process. For optimum FET performance, a 1–2-nm h-BN crystal would be used, instead of the 3.5 nm used here. The substrate (or bottom) h-BN crystal is also shared among the devices and is 15-nm thick. The contact resistance for these devices is about ~200 Ω-μm from the metal-graphene edge contact. About ~200 Ω of resistance (measured from a comparable device) is added by the leads connecting to the device. For the devices with L_G below 200 nm, there is little difference in the output characteristics, which suggests ballistic transport. The nonsaturating current characteristics in these ballistic devices are due to the ambipolar nature of the graphene channel [16]. The minimum g_{ds} and maximum g_m values of these short-channel devices are 300 and 600 μS/μm [Fig. 2(b)], respectively, while the long-channel device (1.2 μm) has a minimum g_{ds} value of 70 μS/μm and maximum g_m value of 500 μS/μm.

To understand these characteristics in more detail, it is useful to fit these to a physically motivated compact model. While gradual channel approximation models have been used quite successfully to model the long-channel GFETs [16], [29], they are a less useful starting point for the devices primarily characterized by ballistic transport [30]. A virtual source (VS) model is valid for both long-channel drift-diffusion transport and short-channel ballistic transport [31]. In this approach, the current is modeled as

$$\frac{I_D}{W} = (Q_{x0e} + Q_{xh0})\, v_{x0} F_{sat} \tag{1}$$

$$F_{sat} = \frac{V'_{DS}/V_{sat}}{(1 + (V'_{DS}/V_{sat})^{1/\beta})^{\beta}} \tag{2}$$

$$V_{sat} = \frac{L_G v_{x0}}{\mu} \tag{3}$$

$$Q_{x0e(h)} = \int_0^\infty 8\pi \frac{E}{(hv_F)^2} \frac{1}{1 + e^{(E+E_{cs(d)})/k_B T}}\, dE \tag{4}$$

$$C_Q \approx C_{Qi} \sqrt{1 + \left(\frac{E_c}{k_B T \ln(4)}\right)^2} \tag{5}$$

where I_D is the drain current, W is the device width, and Q_{x0e} and Q_{x0h} are the areal electron and hole charge densities, respectively, at the virtual drain and source [31], [32]. v_{x0} is the carrier injection velocity and F_{sat} is an empirical function used to transition between the linear and saturated transport regimes [31], [33]. β is a fitting parameter which is 2 ± 0.1 for all devices. V'_{DS} is the intrinsic drain–source voltage of the GFET, which removes the effects of source and drain contact resistance. E_{cs} and E_{cd} are the local energy potentials at the VS and drain. C_Q is the quantum capacitance and C_{Qi} is a constant 8.426 fF/μm^2 [34].

IV. Analysis

The resulting VS model is used to perform a least-squares fit to the experimentally measured data [Fig. 2(a)], determining both the mobility [μ, Fig. 2(e)] and the carrier injection velocity [v_{x0}, Fig. 2(d)] as a function of L_G. From this parameter extraction, we find that the mobility decreases with decreasing L_G due to the onset of ballistic transport. The mobility can be estimated by

$$\frac{1}{\mu} = \frac{\lambda_{mfp}}{\mu_{eff}} \frac{1}{L_G} + \frac{1}{\mu_{eff}} \tag{6}$$

where λ_{mfp} is the mean-free-path and μ_{eff} is the effective mobility for a device dominated by drift-diffusion transport with L_G much larger than λ_{mfp} [31], [35], [36]. This model is derived from the Landauer formulation [37] and applies in the region of linear response, matching other approaches commonly employed to characterize the mean-free-path from measured conductivity [9]. Fig. 3(a) shows $1/\mu$ as a function

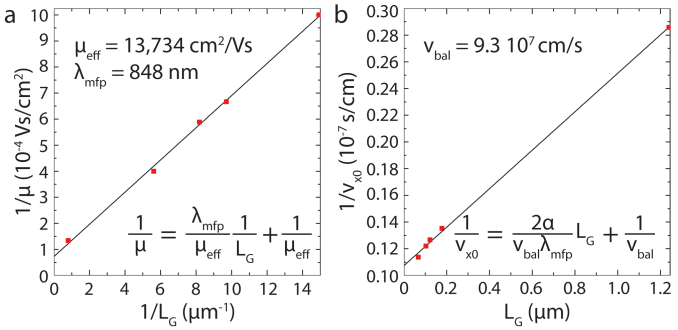

Fig. 3. (a) Scatter plot of the linear relationship between the inverse of the extracted mobility with the inverse of the gate length for the devices in Fig. 2. This gives a linearly extrapolated effective mobility and mean-free-path of 13 734 cm^2/Vs and 848 nm, respectively. (b) Linear relationship between the inverse of the injection velocity and gate length for the same devices in (a). The extrapolation indicates a ballistic velocity of 9.3×10^7 cm/s or 93% of the Fermi velocity.

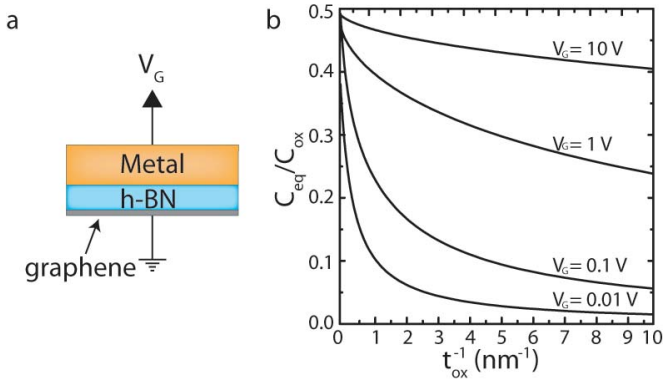

Fig. 4. (a) Schematic for a MIG capacitor. (b) Ratio of the equivalent series capacitance, C_{eq} and the geometric, oxide capacitance, C_{ox} as a function of t_{ox} for fixed-gate biases of 0.01, 0.1, 1, and 10 V.

of $1/L_G$. By employing a linear fit to the data, we determine a λ_{mfp} of 848 nm and a μ_{eff} of 13 734 cm^2/Vs. The source-injection velocity is similarly given by

$$\frac{1}{v_{x0}} = \frac{2\alpha}{v_{bal}\lambda_{mfp}} L_G + \frac{1}{v_{bal}} \tag{7}$$

where v_{bal} is the ballistic velocity and α is a dimensionless constant of proportionality [26], [30], [31]. Here, we assume that the mean-free-path determined by the length dependence of the mobility in the linear regime is equal to that determined by the velocity dependence in the saturated regime, which is a common assumption in these models [26], [30], [31]. Fig. 3(b) shows $1/v_{x0}$ as a function of L_G, which determined a v_{bal} of 9.3×10^7 cm/s, very close to the Fermi velocity of graphene, $1 \pm 0.05 \times 10^8$ cm/s [38].

The extracted λ_{mfp} indicates that all the devices measured in Fig. 2 are ballistic except for the 1.24-μm channel-length device. To the best of our knowledge, these GFETs are the first to demonstrate essentially the ballistic transport at channel lengths in excess of 0.5 μm. The effective mobility is also among the largest reported for a GFET due to the high-quality h-BN/graphene heterostructures. However, these values of mean-free-path and effective mobility are lower than what has been reported for h-BN/graphene heterostructures under low bias [32]. The thinner BN gate dielectrics employed here, as well as the additional processing required to produce the more complex FET structures, are probably resulting in some reduction in encapsulated graphene channel quality. The ballistic velocity achieved in these devices, limited by the Fermi velocity in graphene, is more than five times the band-structure-limited ballistic velocities observed in CMOS devices [39].

Despite the higher carrier velocity and mobility, the g_m and g_{ds} values of these devices are significantly lower than those of silicon devices at comparable channel lengths, due to the effects of quantum capacitance, C_Q, and ambipolar channel conduction. The g_m value is proportional to the effective gate capacitance (C_{eq}), which for a metal–insulator–graphene (MIG) capacitor [Fig. 4(a)] is the series combination of the electrostatic capacitance (C_{ox}) and the quantum capacitance, $C_{eq} = C_{ox}C_Q/(C_{ox} + C_Q)$ [Fig. 4(b)]. Fig. 4(b) shows the ratio C_{eq} to C_{ox} as a function of h-BN thickness (t_{ox}) for different fixed-gate biases, indicating that the quantum capacitance prevents C_{eq} from being reduced below C_Q. C_Q is on the order of 1 μF/cm^2 and halves C_{eq} from the electrostatic C_{ox} value at a t_{ox} of 1 nm. In contrast, silicon CMOS exhibits a C_Q of ~134 μF/cm^2, 16 times larger than in graphene [40], giving $C_{eq} \sim C_{ox}$ for silicon for any achievable EOT. By using high-k gate dielectrics, others have been able to reduce the EOT below that achieved in this paper. For example, graphene transistors exhibiting a g_m of 1.2 mS/μm have been demonstrated using 4-nm HfO_2 [41]. However, silicon devices, with significantly lower carrier velocities and mobilities exhibit $g_m > 2$ mS/μm [42] for channel length below 65 nm because the silicon devices are not limited by quantum capacitance.

Another fundamental limitation is the zero bandgap of graphene, which limits the achievable g_{ds}. When $V'_{DS} > V'_{GS} - V_{Dirac}$, the drain begins injecting a substantial hole current, giving rise to the second linear regime in the GFET I–V characteristic, and increasing g_{ds} [16]. Here, V'_{DS} is the intrinsic source–drain bias, V'_{GS} is the intrinsic gate–source bias, both ignoring the effects of contact resistance, and V_{Dirac} is the Dirac voltage. As a result, the minimum g_{ds} value occurs in a narrow regime of drain biases in which the electron current has saturated but hole densities are not yet substantial. The g_{ds} values for the short-channel GFETs considered here are on the order of 300 μS/μm, more than three times what is typical for 65-nm silicon devices. In addition, since silicon devices are unipolar, the region of drain biases for which this g_{ds} value is valid is much larger than for GFETs.

V. Conclusion

This paper demonstrates the ballistic short-channel GFETs with EOT of less than 3.5 nm, which exhibit among the highest achieved mobilities and carrier velocities. Ballistic behavior is observed with mean-free-paths in excess of 800 nm, even at high biases, opening up intriguing possibilities for devices based on ballistic transport over longer length scales. For example, devices based on electron focusing can be achieved

at room temperature in graphene [43]. Nevertheless, as an FET channel material, despite carrier velocities that are more than a factor of four greater than those achievable in silicon, the ambipolar conduction and quantum capacitance of graphene are the fundamental limitations of the graphene itself, producing g_m and g_{ds} characteristics that are substantially worse than in comparable silicon CMOS devices.

REFERENCES

[1] R. Cheng *et al.*, "High-frequency self-aligned graphene transistors with transferred gate stacks," *Proc. Nat. Acad. Sci. USA*, vol. 109, no. 29, pp. 11588–11592, 2012.

[2] L. Liao *et al.*, "High-speed graphene transistors with a self-aligned nanowire gate," *Nature*, vol. 467, pp. 305–308, Sep. 2010.

[3] Y.-M. Lin *et al.*, "100-GHz transistors from wafer-scale epitaxial graphene," *Science*, vol. 327, no. 5966, p. 662, 2010.

[4] I. Meric *et al.*, "High-frequency performance of graphene field effect transistors with saturating IV-characteristics," in *Proc. IEEE IEDM*, Dec. 2011, pp. 2.1.1–2.1.4.

[5] J. Lee *et al.*, "25 GHz embedded-gate graphene transistors with high-κ dielectrics on extremely flexible plastic sheets," *ACS Nano*, vol. 7, no. 9, pp. 7744–7750, 2013.

[6] W. Zhu *et al.*, "Graphene radio frequency devices on flexible substrate," *Appl. Phys. Lett.*, vol. 102, no. 23, p. 233102, 2013.

[7] N. Petrone, I. Meric, T. Chari, K. L. Shepard, and J. Hone, "Graphene field-effect transistors for radio-frequency flexible electronics," *IEEE J. Electron Devices Soc.*, vol. 3, no. 1, pp. 44–48, Jan. 2015.

[8] N. Petrone, I. Meric, J. Hone, and K. L. Shepard, "Graphene field-effect transistors with gigahertz-frequency power gain on flexible substrates," *Nano Lett.*, vol. 13, no. 1, pp. 121–125, 2013.

[9] L. Wang *et al.*, "One-dimensional electrical contact to a two-dimensional material," *Science*, vol. 342, no. 6158, pp. 614–617, 2013.

[10] K. I. Bolotin *et al.*, "Ultrahigh electron mobility in suspended graphene," *Solid State Commun.*, vol. 146, nos. 9–10, pp. 351–355, 2008.

[11] C. Lee, X. Wei, J. W. Kysar, and J. Hone, "Measurement of the elastic properties and intrinsic strength of monolayer graphene," *Science*, vol. 321, no. 5887, pp. 385–388, 2008.

[12] F. Xia, D. B. Farmer, Y.-M. Lin, and P. Avouris, "Graphene field-effect transistors with high on/off current ratio and large transport band gap at room temperature," *Nano Lett.*, vol. 10, no. 2, pp. 715–718, 2010.

[13] W. Liu *et al.*, "High-performance few-layer-MoS_2 field-effect-transistor with record low contact-resistance," in *Proc. IEEE IEDM*, Dec. 2013, pp. 19.4.1–19.4.4.

[14] G. Fiori, D. Neumaier, B. N. Szafranek, and G. Iannaccone, "Bilayer graphene transistors for analog electronics," *IEEE Trans. Electron Devices*, vol. 61, no. 3, pp. 729–733, Mar. 2014.

[15] J. S. Moon *et al.*, "Lateral graphene heterostructure field-effect transistor," *IEEE Electron Device Lett.*, vol. 34, no. 9, pp. 1190–1192, Sep. 2013.

[16] I. Meric, M. Y. Han, A. F. Young, B. Ozyilmaz, P. Kim, and K. L. Shepard, "Current saturation in zero-bandgap, top-gated graphene field-effect transistors," *Nature Nanotechnol.*, vol. 3, no. 11, pp. 654–659, 2008.

[17] Y. Wu *et al.*, "State-of-the-art graphene high-frequency electronics," *Nano Lett.*, vol. 12, no. 6, pp. 3062–3067, 2012.

[18] H. Wang, Y. Wu, C. Cong, J. Shang, and T. Yu, "Hysteresis of electronic transport in graphene transistors," *ACS Nano*, vol. 4, no. 12, pp. 7221–7228, 2010.

[19] J. Niinistö *et al.*, "Controlled growth of HfO_2 thin films by atomic layer deposition from cyclopentadienyl-type precursor and water," *J. Mater. Chem.*, vol. 15, no. 23, pp. 2271–2275, 2005.

[20] F. Xia, V. Perebeinos, Y.-M. Lin, Y. Wu, and P. Avouris, "The origins and limits of metal–graphene junction resistance," *Nature Nanotechnol.*, vol. 6, no. 3, pp. 179–184, 2011.

[21] E. Watanabe, A. Conwill, D. Tsuya, and Y. Koide, "Low contact resistance metals for graphene based devices," *Diamond Rel. Mater.*, vol. 24, pp. 171–174, Apr. 2012.

[22] H. Xu, S. Wang, Z. Zhang, Z. Wang, H. Xu, and L.-M. Peng, "Contact length scaling in graphene field-effect transistors," *Appl. Phys. Lett.*, vol. 100, no. 10, p. 103501, 2012.

[23] K. Nagashio, T. Nishimura, K. Kita, and A. Toriumi, "Contact resistivity and current flow path at metal/graphene contact," *Appl. Phys. Lett.*, vol. 97, no. 14, p. 143514, 2010.

[24] C. R. Dean *et al.*, "Boron nitride substrates for high-quality graphene electronics," *Nature Nanotechnol.*, vol. 5, no. 10, pp. 722–726, 2010.

[25] H. Wang *et al.*, "BN/graphene/BN transistors for RF applications," *IEEE Electron Device Lett.*, vol. 32, no. 9, pp. 1209–1211, Sep. 2011.

[26] I. Meric, C. R. Dean, A. F. Young, J. Hone, P. Kim, and K. L. Shepard, "Graphene field-effect transistors based on boron nitride gate dielectrics," in *Proc. IEEE Int. Electron Devices Meeting*, Dec. 2010, pp 23.2.1–23.2.4.

[27] J. S. Moon, "Ultra-low resistance ohmic contacts in graphene field effect transistors," *Appl. Phys. Lett.*, vol. 100, no. 20, pp. 203512-1–203512-3, 2012.

[28] A. F. Young *et al.*, "Electronic compressibility of layer-polarized bilayer graphene," *Phys. Rev. B*, vol. 85, no. 23, pp. 235458-1–235458-5, 2012.

[29] S. A. Thiele, J. A. Schaefer, and F. Schwierz, "Modeling of graphene metal-oxide-semiconductor field-effect transistors with gapless large-area graphene channels," *J. Appl. Phys.*, vol. 107, no. 9, pp. 094505-1–094505-8, 2010.

[30] L. Wei, O. Mysore, and D. A. Antoniadis, "Virtual-source-based self-consistent current and charge FET models: From ballistic to drift-diffusion velocity-saturation operation," *IEEE Trans. Electron Devices*, vol. 59, no. 5, pp. 1263–1271, May 2012.

[31] S. Rakheja, Y. Wu, H. Wang, T. Palacios, P. Avouris, and D. A. Antoniadis, "An ambipolar virtual-source-based charge-current compact model for nanoscale graphene transistors," *IEEE Trans. Nanotechnol.*, vol. 13, no. 5, pp. 1005–1013, Sep. 2014.

[32] A. Khakifirooz, O. M. Nayfeh, and D. A. Antoniadis, "A simple semiempirical short-channel MOSFET current–voltage model continuous across all regions of operation and employing only physical parameters," *IEEE Trans. Electron Devices*, vol. 56, no. 8, pp. 1674–1680, Aug. 2009.

[33] S. Rakheja, H. Wang, T. Palacios, I. Meric, K. L. Shepard, and D. A. Antoniadis, "A unified charge-current compact model for ambipolar operation in quasi-ballistic graphene transistors: Experimental verification and circuit-analysis demonstration," in *Proc. IEEE Int. Electron Devices Meeting*, Dec. 2013, pp. 5.5.1–5.5.4.

[34] K. N. Parrish, M. E. Ramón, S. K. Banerjee, and D. A. Akinwande, "A compact model for graphene FETs for linear and non-linear circuits," in *Proc. SISPAD*, 2012, pp. 75–78.

[35] A. Majumdar and D. A. Antoniadis, "Analysis of carrier transport in short-channel MOSFETs," *IEEE Trans. Electron Devices*, vol. 61, no. 2, pp. 351–358, Feb. 2014.

[36] M. S. Lundstrom, "On the mobility versus drain current relation for a nanoscale MOSFET," *IEEE Electron Device Lett.*, vol. 22, no. 6, pp. 293–295, Jun. 2001.

[37] S. Datta, *Electronic Transport in Mesoscopic Systems*. Cambridge, U.K.: Cambridge Univ. Press, 1995.

[38] M. Sprinkle *et al.*, "First direct observation of a nearly ideal graphene band structure," *Phys. Rev. Lett.*, vol. 103, pp. 226803-1–226803-4, Nov. 2009.

[39] Y. Liu, M. Luisier, A. Majumdar, D. A. Antoniadis, and M. S. Lundstrom, "On the interpretation of ballistic injection velocity in deeply scaled MOSFETs," *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 994–1001, Apr. 2012.

[40] S. Luryi, "Quantum capacitance devices," *Appl. Phys. Lett.*, vol. 52, no. 6, pp. 501–503, 1988.

[41] S.-J. Han, K. A. Jenkins, A. V. Garcia, A. D. Franklin, A. A. Bol, and W. Haensch, "High-frequency graphene voltage amplifier," *Nano Lett.*, vol. 11, no. 9, pp. 3690–3693, 2011.

[42] C. C. Wu *et al.*, "High performance 22/20 nm FinFET CMOS devices with advanced high-*K*/metal gate scheme," in *Proc. IEEE IEDM*, Dec. 2010, pp. 27.1.1–27.1.4.

[43] V. V. Cheianov, V. Fal'ko, and B. L. Altshuler, "The focusing of electron flow and a Veselago lens in graphene *p-n* junctions," *Science*, vol. 315, no. 5816, pp. 1252–1255, 2007.

Authors' photographs and biographies not available at the time of publication.