Magnetic Thin-Film Inductors for Monolithic Integration with CMOS

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Abstract

This paper presents the fabrication, design and electrical performance of magnetic thin-film inductors for monolithic integration with CMOS for DC-DC power conversion. Magnetic core inductors were fabricated using conventional CMOS processes to achieve peak inductance density of 290nH/mm^2, quality factor 15 at 150MHz, current density exceeding 11A/mm^2 and coupling coefficient of 0.89 for coupled inductors.

Introduction

The introduction of high permeability magnetic thin-films to CMOS manufacturing provides a new class of integrated inductor, enabling higher levels of integration and performance for applications that are currently relegated to using discrete inductors. Integrated magnetic thin-film inductors incorporate high permeability (μ_{Rel} > 500), low coercivity (H_C < 1 Oe) magnetic materials to provide a low reluctance path for the coil's magnetic flux, generating a significant inductance enhancement [1-4] relative to air-core inductors. These inductors can be fabricated with standard CMOS manufacturing processes and have a low profile (< 30µm), which makes them compatible for monolithic integration with CMOS ICs as a back-end process option (Figs. 1,2). The inductors presented here exhibit high inductance for a broad frequency band (> 1 GHz), high current density and low DC resistance relative to existing on-chip inductor technologies. These inductors will enable a new set of IC applications such as monolithically integrated voltage regulation (MIVR), where all components of a switched inductor DC-DC power converter are integrated on-chip. Integrated voltage regulation allows power to be delivered to ICs at higher voltages and then efficiently down converted on-chip, reducing I^2R loss in the power delivery network, and enabling improved power management with a larger number of independently scalable on-chip power supplies [5-8].

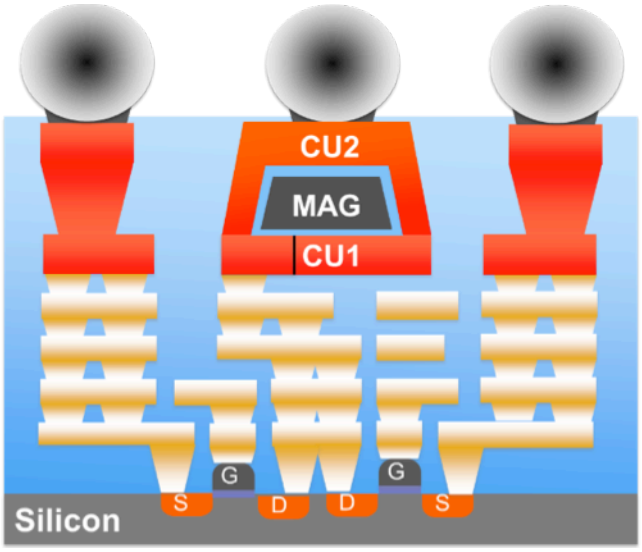

Fig.1 Illustrated cross section of magnetic thin-film inductors monolithically integrated with CMOS IC

Fabrication of Magnetic Thin-Film Inductors

Magnetic thin-film inductors were fabricated at TSMC on 300mm wafers in a pilot manufacturing line using standard CMOS manufacturing equipment and processes. Fig. 1 illustrates the cross section of the inductors integrated with a CMOS IC, Fig. 2 is an SEM cross section of the same. The inductor consists of three metal layers separated by insulators. The inductor coil is formed from copper interconnect layers CU1 and CU2. CU1 is planar while CU2 is non-planar and connects to CU1 through openings in insulating layers. The magnetic core layer is MAG. For characterization, inductors were fabricated on a test vehicle that includes only relevant inductor layers (CU1, MAG, CU2, insulators). Magnetic thin-film inductors have also been fabricated on 300mm CMOS wafers at TSMC. Passivation and wafer finishing steps necessary for commercial CMOS wafers were completed on the test vehicle wafers and consequently the performance demonstrated on the test vehicle will be consistent with inductors fabricated on commercial CMOS wafers.

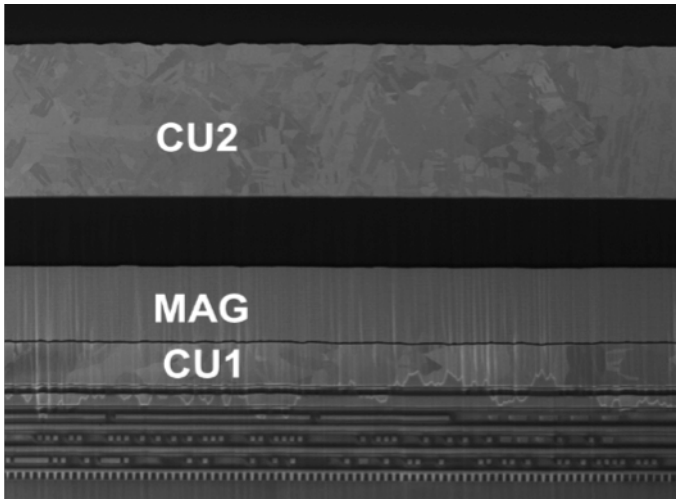

Fig.2 SEM cross section of magnetic thin-film inductors monolithically integrated with CMOS IC

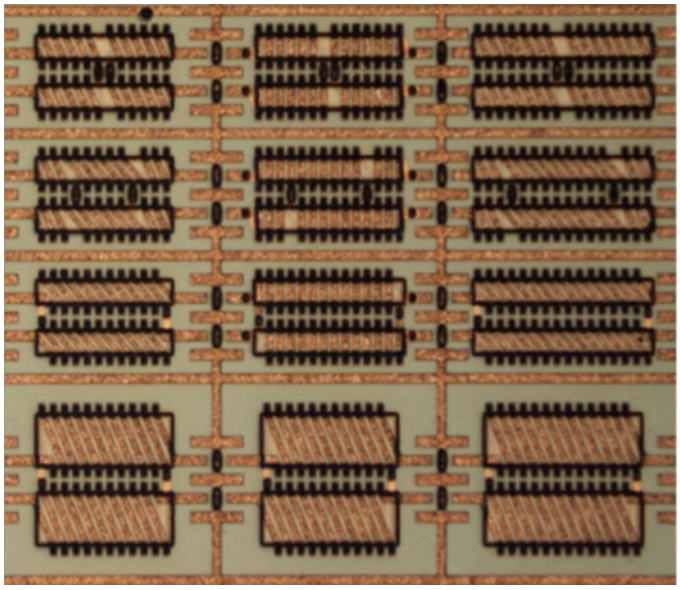

Fig.3 Microscope image of magnetic thin-film inductors as fabricated on test vehicle

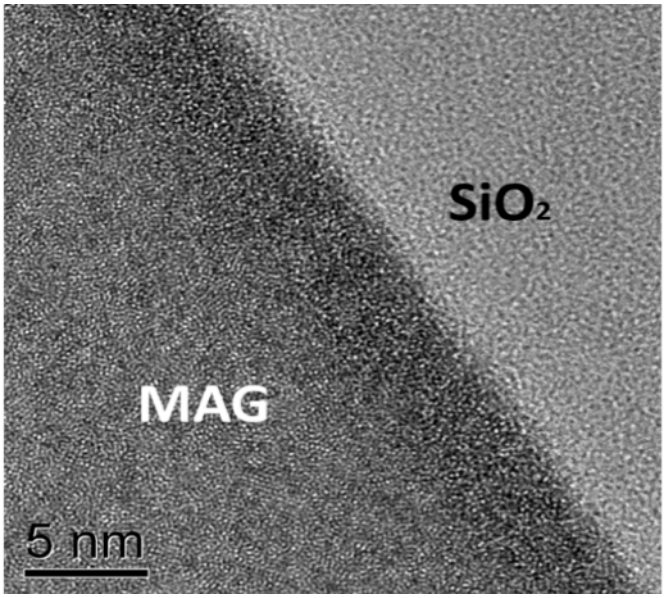

Fig.4 High magnitude TEM cross-sectional view, the MAG layer is amorphous.

Design of Magnetic Thin-Film Inductors

Inductors were designed and fabricated on a test vehicle (Fig. 3). The library of inductor designs includes variations on number of turns, winding width, interleaving for coupled inductors and magnetic core dimensions. The core is a composite of amorphous cobalt alloy (Fig. 4) and insulating laminations (Fig. 5) to suppress eddy currents and improve frequency response. The bulk magnetic core material has an coercivity < 1 0e and saturation field ~25 Oe (Fig. 6). The magnetic thin-film maintains a large real permeability up to ~1.4 GHz, (Fig. 6).

The inductors were designed to be suitable for several applications where monolithic integration with CMOS is advantageous, including integrated DC-DC power conversion. Inductor designs were optimized to achieve high figures of merit: inductance density, current density, peak quality factor and L_{AC}/R_{DC}.

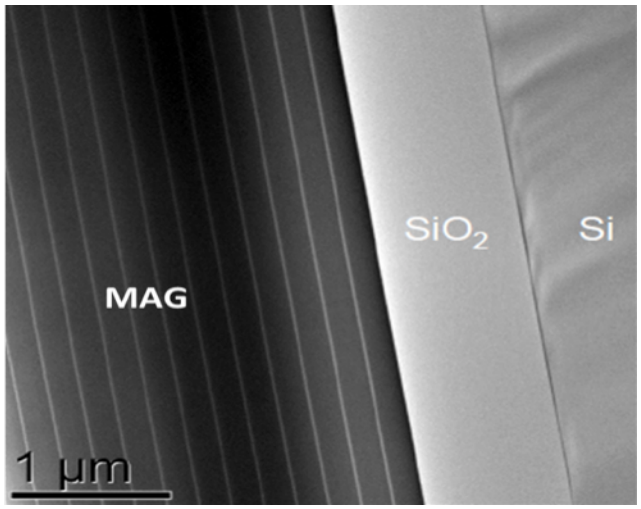

Fig.5 Low magnitude TEM cross-sectional view, the MAG layer is laminated to suppress eddy current.

Electrical Performance of Magnetic Thin-Film Inductors

Inductors were measured with a 4-port vector network analyzer and RF probes. The peak quality factor as a function of inductance density, and inductance per resistance as a function of inductance are shown in Fig. 7 and Fig. 8, respectively, along with several other notable thin-film inductors [1-4]. Air-core inductors with coils similar to the magnetic core inductors have been included for comparison. These inductors achieve a peak quality factor as high as 15 at 150 MHz and a maximum inductance density of 290 nH/mm^2. Our inductors are among the highest performing in this class, with a high inductance density and quality factor, trending towards the upper right corner of Fig. 7. Our inductors also achieve a low DC resistance, making them suitable for applications with large DC currents, such as power conversion. The inductors achieve a maximum L_{AC}/R_{DC} of

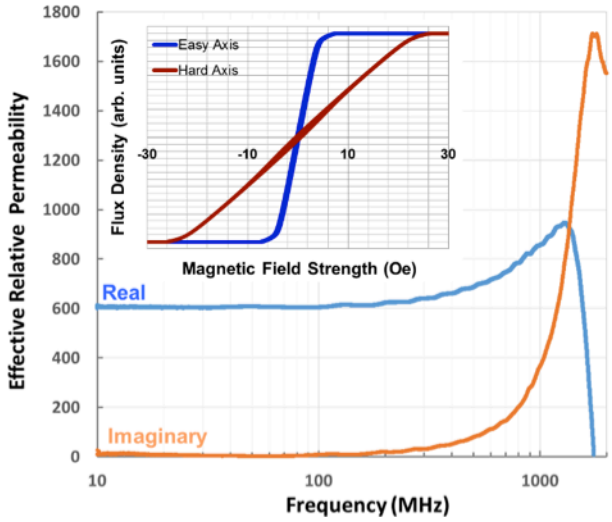

Fig.6 Real and imaginary components of relative permeability for magnetic thin-film. INSET: BH Loop for magnetic film

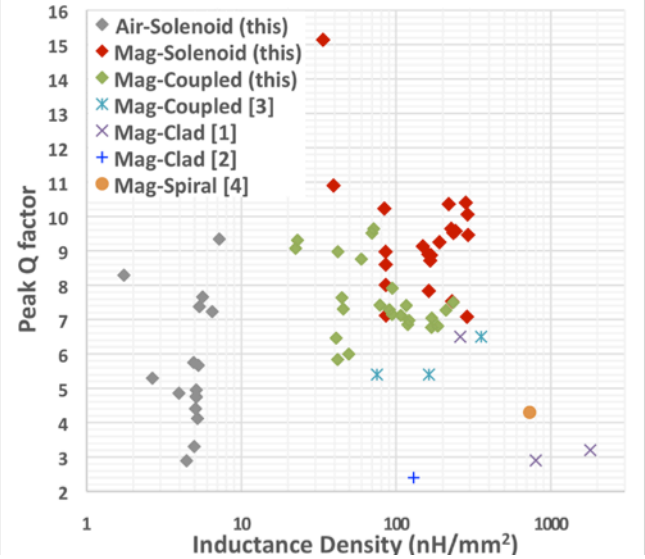

Fig.7 Peak Quality Factor vs. Inductance Density of integrated inductors on silicon substrates

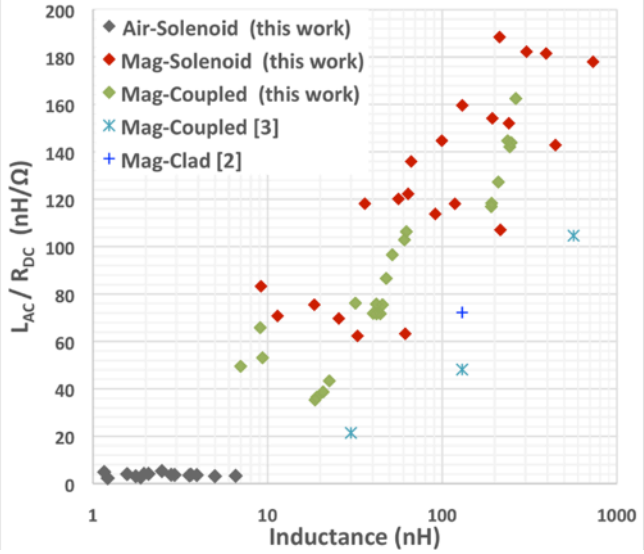

Fig.8 Inductance/Resistance vs. Inductance of integrated inductors on silicon substrates

188 nH/Ω with an inductance of 212 nH, and achieve the best L_{AC}/R_{DC} ratio for a wide range of inductance values (Fig. 8).

The inductance versus frequency for several inductor designs is shown in Fig. 9. A wide range of inductance (1 nH – 730 nH), resistance (0.04 Ω – 4.1 Ω) and coupling (0.25 – 0.89) values are exhibited. The inductance for most devices falls off rapidly at the self-resonant frequency, where the device inductance and parasitic capacitance resonate.

The inductance for a single solenoid inductor is shown in Fig. 10 as a function of a DC current that is superimposed onto the AC measurement signal. The magnetic core material will saturate with large applied magnetic fields and consequently with large currents in the inductor coil. The onset of magnetic saturation occurs at 450 mA with 10% inductance degradation for the device represented in Fig. 10. The inductor saturation current is dependent on most design parameters, but especially on the number of turns for the inductor coil, with more coil turns resulting in a lower saturation current.

A contour plot of inductance for a coupled inductor with coupling coefficient of ~0.85 is shown in Fig. 11a, with corresponding coupling plot for coupling coefficient in Fig. 11b. This device achieves a current density > 12 A/mm^2 when the currents through inductors 1 and 2 are balanced to within ~900 mA. The impact of magnetic saturation is reduced in inversely coupled inductors when similar currents pass through each of the inductor coils and the induced magnetic field from each coil cancels, to reduce the net field imposed on the magnetic core. The inductance and coupling coefficient contour plots from Fig. 12 represent a similar coupled inductor as Fig. 11, but with smaller coupling coefficient and consequently higher susceptibility to magnetic saturation. The use of inversely coupled inductors has been

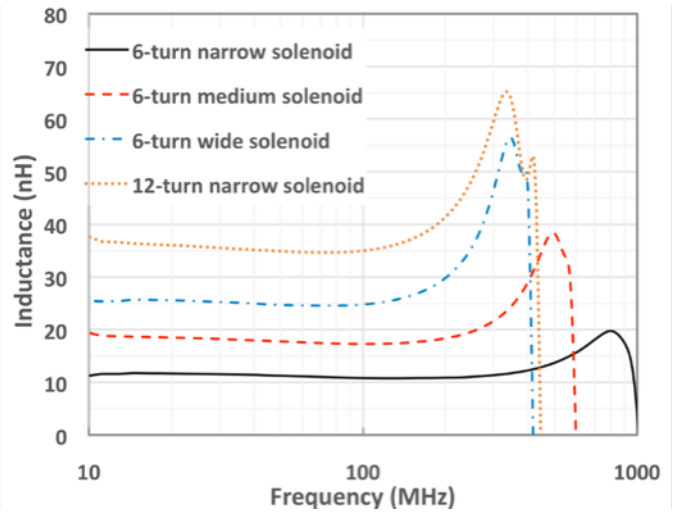

Fig.9 Inductance vs. Frequency of integrated inductors on silicon substrates

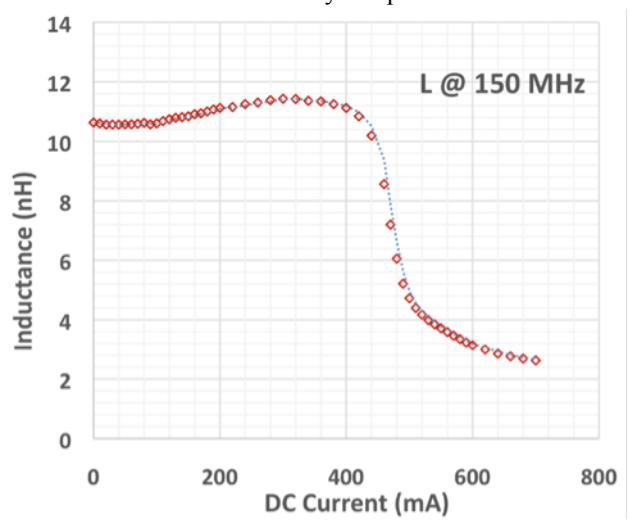

Fig.10 Inductance vs. DC Current for a single magnetic thin-film solenoid inductor

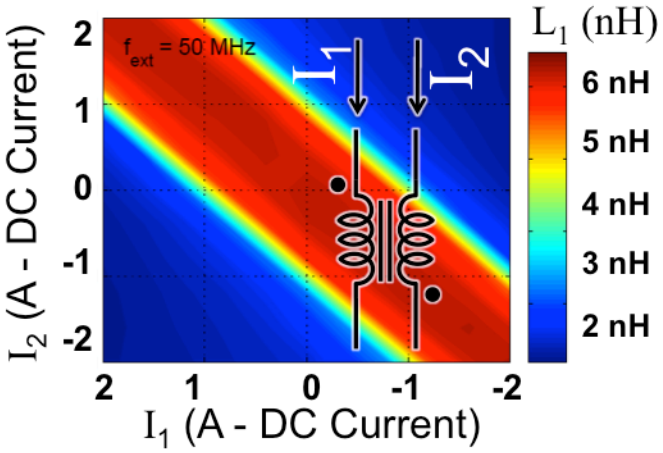

Fig.11a Contour plot showing average inductance for a coupled inductor with independent average inductor currents

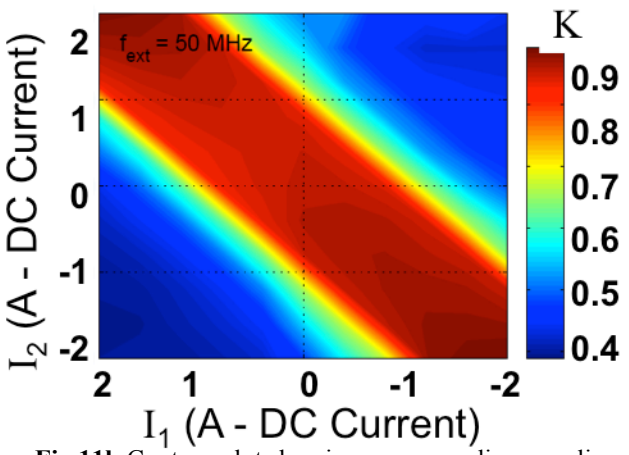

Fig.11b Contour plot showing corresponding coupling coefficient for inductor from Fig.11a

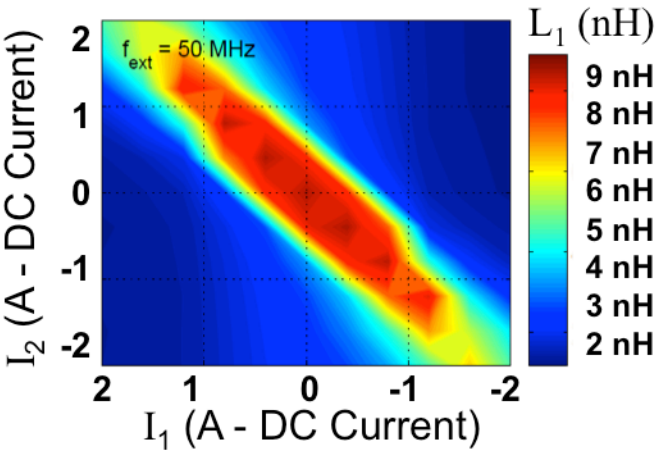

Fig.12a Contour plot showing average inductance for a coupled inductor with independent average inductor currents

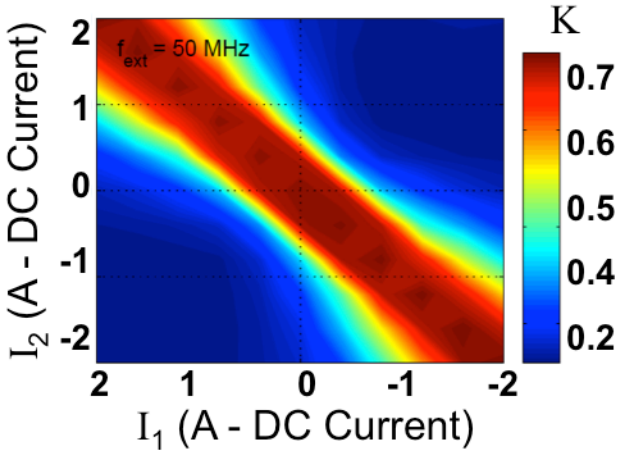

Fig.12b Contour plot showing coupling coefficient for inductor from Fig.12a. **Note**: lower coupling coefficient than the inductor represented in Fig.11b

proven to effectively reduce the impact of magnetic saturation, in addition to reducing inductor current ripple and improving regulation bandwidth in multi-phase interleaved buck converters [7,8].

The performance achieved with the inductors presented here indicates that these inductors are suitable for many applications when integrated with CMOS, including integrated power conversion with high current density and conversion efficiency. Future design and process enhancements are expected to improve inductance density, quality factor, DC resistance and bandwidth to increase the set of applications where this class of inductor can be effectively utilized.

Acknowledgement

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