

An 82%-Efficient Multiphase Voltage-Regulator 3D Interposer with On-Chip Magnetic Inductors

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Abstract. This paper presents a three-dimensional (3D) fully integrated high-speed multiphase voltage regulator. A complete switched-inductor regulator is integrated with a four-plane NoC in a two-high chip stack combining integrated magnetics, through-silicon vias (TSVs), and 45-nm SOI CMOS devices. Quasi- V^2 hysteretic control is implemented over eight injection-locked fixed-frequency phases to achieve fast response, steady-state regulation, and fixed switching frequency. Peak efficiency of 82% for conversion from 1.66 V to 0.83 V is observed at a 150 MHz per-phase switching frequency. This is the first demonstration of high-speed voltage regulation using on-chip magnetic-core inductors in a 3D stack and achieves sub- μ s dynamic supply voltage scaling for high-density embedded processing applications.

Keywords: buck converter, integrated magnetics, 3D integration, TSVs, nonlinear control, DVFS.

Introduction. Switched-inductor-based DC-DC converters are the preferred approach for generating the myriad supply voltages required for electronic systems due to their high efficiency, variable conversion ratios, and power-handling capabilities. These converters, however, have defied integration and scaling due to the requirement for inductors with high quality factors, inductance densities, and current-carrying capabilities. Thus far, these operating parameters have been met using off-chip discrete inductors. Due to the issues of integration density and scaling-up of voltage domain count, off-chip regulation makes it challenging to maintain power signal integrity, especially given the scaling of supply voltage and increasing transient load demands. In particular, discrete components dominate board area, and the design of the board-level power distribution network (PDN) to mitigate inductive droop and resistive loss becomes increasingly constrained. Furthermore, communication with off-chip regulators does not occur quickly enough to realize dynamic voltage and frequency scaling (DVFS) on the time scale of workload changes that characterize state-of-the-art multi-core systems-on-chip. Spatially and temporally granular DVFS promises large improvements in energy efficiency of CMOS logic chips [1][2].

Chip-stacked voltage regulators. Integrating voltage regulators on the load die addresses the PDN and DVFS challenges. However, the low realizable quality factor of air-core on-chip inductors necessitates package integration instead [2], the use of which limits the scalability of these approaches. In this work, we use integrated magnetic materials to achieve CMOS-compatible power inductors with Q s of more than 6 at 10 MHz and inductance densities of more than 130 nH/mm² (compare to package inductors at typically 4-40 nH/mm² [3]). These inductors are placed on an interposing die mated with TSVs between a scaled CMOS processor in 45-nm SOI technology and a laminate ball-grid-array (BGA) package (Fig. 1). This heterogeneous integration decouples the

fabrication concerns of the processor from those of magnetic layer deposition and TSV construction. The planar-area reuse inherent in 3D stacking aids scaling of the number of voltage domains relative to package-integrated inductors, due to higher density and reduced integration complexity.

Interposer Design and Fabrication. Electroplating is an important technique for the deposition of thick metal films due to its high deposition rate, conformal coverage and low cost, and was thus used for inductor fabrication [4]. Each magnetic inductor consists of electroplated 5 μ m Cu coils enclosed by electroplated 1 μ m Ni₄₅Fe₅₅ yokes. Ni₄₅Fe₅₅ is chosen over Ni₈₀Fe₂₀ for its higher magnetic moment (\sim 1.6 T), high anisotropy field, and higher electrical resistivity (\sim 40 μ Ω -cm). The TSV technology is a TiN/W, insulated-via process that is additionally CMOS-compatible [5].

Representative device data is shown in Fig. 2. The low DC resistance ($< 0.2 \Omega$) ensures conduction losses are kept at a minimum. Frequency-dependent losses (at $f > 100$ MHz) are due to core hysteresis and eddy currents and can be further improved by laminating the magnetic materials with insulators.

The inductors are designed as eight single-turn inductors, coupled pairwise negatively with target $k = 0.4$ to increase saturation current limits. The full interposer layout is shown in Fig. 3. The inductor-to-regulator connections are designed to minimize PDN loss.

Voltage regulator and load design. A single phase of the switched-inductor regulator is shown in Fig. 4. In order to achieve high-speed transient response to voltage-change commands and load current steps, a fixed-frequency variant of quasi- V^2 hysteretic control [6] is used, combining a nonlinear hysteretic control system with a linear proportional-integral (PI) controller for steady-state regulation. The inductor current ripple is sensed indirectly with an RC network across the inductor, and a hysteretic comparator adjusts the switch network to push/pull energy to/from the load as needed. The bang-bang characteristic of the hysteretic controller provides for fast response to load transients and voltage steps.

An injection-locking scheme fixes the normally load-dependent switching frequency of a hysteretic converter and interleaves the eight phases. In steady-state, a digital pulse width modulation (DPWM) block generates a fixed frequency square wave at $f_{sw} = 150$ MHz, V_{PWM} , with duty cycle commensurate with the desired output voltage command as determined by the proportional-integral (PI) control action on V_{CTRL} . V_{PWM} is passed through a one-section RC low-pass filter to generate a reference voltage, V_{HREF} , for the hysteretic control block. Due to the non-zero high frequency rejection, V_{HREF} contains a component at f_{sw} . The oscillations of the hysteretic controller can thus be induced to lock to f_{sw} so long as the injected signal is at higher frequency than the free-running hysteretic oscillation (Fig. 5). An inductor current

transient will perturb the lock, allowing for high-speed nonlinear feedback correction. All eight phases of the converter can be steady-state synchronized with interleaved phase by controlling the DPWM waveform phases.

A digital circuit load consisting of a four-plane network-on-chip (NoC) is integrated on the same silicon die as the controller in a use case mimicking DVFS architectures for modern embedded applications. The four NoC planes operate in parallel, each with an independent clock frequency.

The controller chip includes 70 nF of decoupling capacitance occupying 1 mm² on-die.

Chip-stack fabrication and measurement results. The regulator and load are implemented in 45-nm SOI technology, with a maximum regulator input voltage of 1.8 V. Fig. 6 shows the cross-section of the packaged chips. The chip-stack was tested at a 2-to-1 conversion across output voltage and at three switching frequencies. Efficiencies as a function of output voltage and load current are displayed in Fig. 7. A peak efficiency of 82% is seen on conversion from 1.66 V to 0.83 V at 150 MHz per-phase switching frequency and output current of 390 mA. At conversion of 1.8 V to 0.9 V, efficiency drops slightly to 78%. A large signal 0 to 1 V output step response is shown in Fig. 8, and clearly highlights the nonlinear and linear

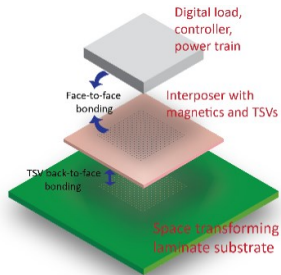


Fig. 1: Chip-stack illustration

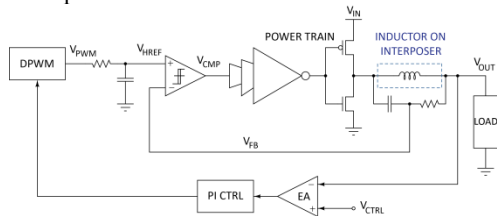


Fig. 4: One phase of the implemented eight-phase regulator

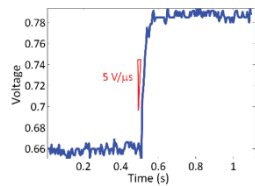


Fig. 9: Small-signal step response

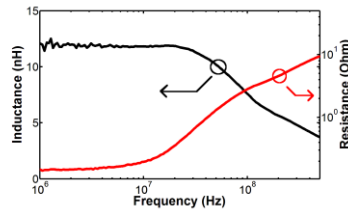


Fig. 2: Representative data for fabricated magnetic-yoke inductors

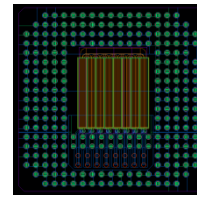


Fig. 3: Interposer layout with TSVs and inductors

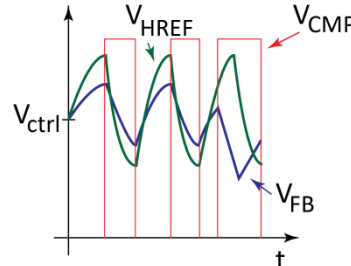


Fig. 5: Two injection-locked periods defined by V_{HREF}, followed by a current transient coupling onto V_{FB}. The employed injection-locking slips and the hysteretic block is able to react asynchronously to the transient.

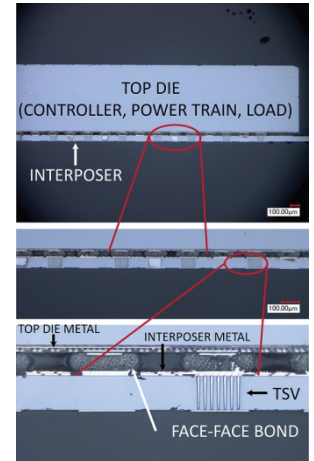


Fig. 6: Three chip-stack cross-sections at increasing zoom

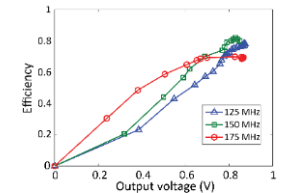
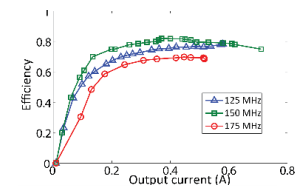


Fig. 7: Efficiency curves

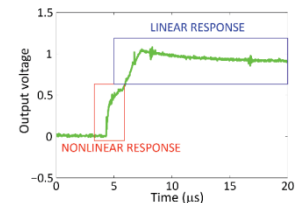


Fig. 8: Large-signal step response

responses of the controller. A 250 mV-change step response (Fig. 9) illustrates a 5 V/μs slew rate, which allows for DVFS at sub-microsecond resolution. The measured steady-state ripple is 20 mV_{pp}, and power density is calculated as 0.9 W/mm². Comparison to previous work is provided in Table 1.

Acknowledgements

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References

[1] Toprak-Deniz, Z. et al., *ISSCC Dig. Tech. Papers*, vol.31, no.2, 2014.
 [2] Burton et al., *APEC*, 2014.
 [3] S. Chickamenahalli et al., *IEEE Trans. Adv. Packaging*, vol.28, no.665, 2005
 [4] N. Wang et al., *J. Appl. Phys.* 111, 07E732, 2012.
 [5] P. Andry et al., *IBM J. Res. Develop.*, 52(6), 571, 2008.
 [6] F. Su, et al., *ISSCC Dig. Tech. Papers*, pp.446-447, 2009.
 [7] H.-P. Le et al., *ISSCC Dig. Tech. Papers*, pp.372-373, 2013.
 [8] C. Huang et al., *IEEE JSSC*, vol.48, no.11, 2013.
 [9] N. Sturcken et al., *ISSCC Dig. Tech. Papers*, pp.400-402, 2012.
 [10] S. Kudva et al., *IEEE JSSC*, vol.46, no.8, 2011.

TABLE I: COMPARISON WITH REPORTED INTEGRATED VOLTAGE REGULATORS

	Energy storage element	Integration type	Peak eff.	Power density @ peak eff. (W/mm ² , over die-stack area)	In/out level @ peak eff. (V/V)
This work	Mag.-core inductor	3D interposer	82%	0.9	1.66/0.83
[7]	On-chip capacitance	Single-die	73%	0.19	4/1
[8]	Bondwire inductor	Package	84.7%	0.148	1.2/0.9
[9]	Mag.-core inductor	2.5D interposer	71%	3.4	1.8/1
[10]	Spiral inductor	Single-die	77%	0.2	1.2/0.88
[2]	Trace inductor	Package	90%	7.9	1.7/1.05