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Complementary Metal-Oxide-Semiconductor Integrated Carbon Nanotube Arrays: Toward Wide-Bandwidth Single-Molecule Sensing Systems

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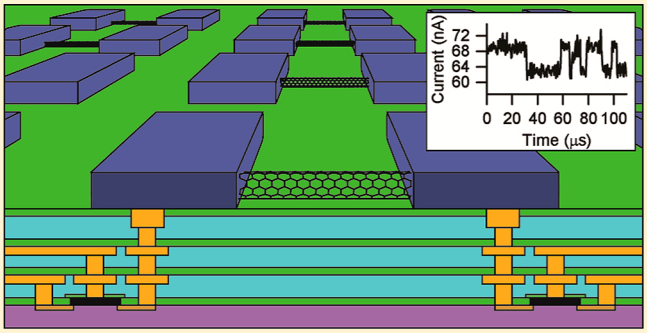
Supporting Information

ABSTRACT: There is strong interest in realizing genomic molecular diagnostic platforms that are label-free, electronic, and single-molecule. One attractive transducer for such efforts is the single-molecule field-effect transistor (smFET), capable of detecting a single electronic charge and realized with a point-functionalized exposed-gate one-dimensional carbon nanotube field-effect device. In this work, smFETs are integrated directly onto a custom complementary metal-oxide-semiconductor chip, which results in an array of up to 6000 devices delivering a measurement bandwidth of 1 MHz. In a first exploitation of these high-bandwidth measurement capabilities, point functionalization through electrochemical oxidation of the devices is observed with microsecond temporal resolution, which reveals complex reaction pathways with resolvable scattering signatures. High-rate random telegraph noise is detected in certain oxidized devices, further illustrating the measurement capabilities of the platform.



KEYWORDS: *Single-molecule, carbon nanotube, CMOS, electrochemical oxidation, random telegraph noise*

Point attachment of single molecules to carbon nanotubes (CNTs) has recently enabled a whole new class of all-electronic label-free single-molecule studies.[1−7] Activities such as lysozyme dynamics,[1] DNA polymerase functionality,[2] and DNA hybridization kinetics[5,6] have been investigated using these single-molecule field-effect transistors (smFETs).

One point functionalization method used to convert a pristine nanotube into a smFET involves electrochemically introducing a defect into the CNT sidewall, which creates a single point of spatially localized charge sensitivity.[5,8] The defect is also used as an attachment point for the covalent binding of a probe molecule, aligning the sensitivity and specificity of the sensor.[5] Current through the nanotube is modulated as the charge density in the vicinity of this sensitive region is altered by a target biomolecule. A typical device configuration is shown in Figure 1, panel a. This exposed-gate device is electrolytically biased by a potential applied through an external reference electrode in the surrounding electrolyte, while a source-drain potential across the device drives the electrical current. Modulations in the current are captured with a transimpedance amplifier.

Charge in the vicinity of the point defect on the CNT is transduced to current levels typically in excess of 10 nA,[5,6,9] which offers the potential to measure single-molecule events with bandwidths at submicrosecond time scales depending on noise sources and parasitics. Additionally, measurements with individual smFETs typically extend over many hours.[5] Direct charged-based sensing in the smFET also obviates the need to perform labeling, simplifying the sample preparation required for single-molecule studies. In contrast, single-molecule fluorescence-based studies with typical fluorescent reporters have signal levels on the order of 5000 photons/s for typical excitation powers,[9,10] limiting temporal resolution to under 1-kHz at tolerable signal-to-noise ratio (SNR).[9] In addition to this limitation in temporal resolution, fluorophores (in oxygen scavenging systems) bleach after only a few minutes of illumination,[10] limiting temporal dynamic range on the high side as well.

smFETs have to-date only been fabricated as discrete devices on passive substrates. The resulting capacitive parasitics, described in more detailed below, increase input-referred current noise at high frequencies, reducing achievable bandwidths. Passive substrates also require coplanar metallization routing, limiting the number of devices that can be fabricated on a single chip.

In this work, we describe the design and postprocessing of a high-bandwidth, complementary metal-oxide-semiconductor (CMOS) integrated smFET array. In addition to a dramatic reduction in the parasitic capacitances of the device and its integration with the transimpedance amplifiers required for current measurement, integration enables large, scalable arrays

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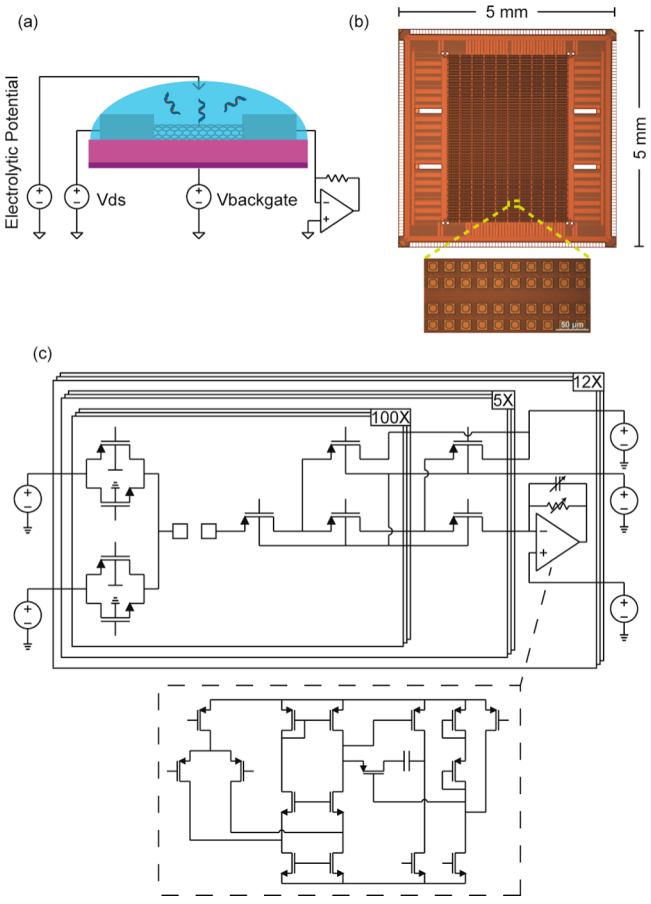

Figure 1. (a) smFET configuration. (b) Image of smFET CMOS chip. (c) Schematic overview of the chip.

of devices, unachievable with passive device array implementations. A CMOS active smFET array will be necessary to achieve the scaled numbers of devices required for many practical applications of smFET technology including genomic assays and sequencing-by-synthesis.[11] In our prototype, integrated nanotubes are electrically characterized to bandwidths of 1 MHz. smFET devices are then created by electrochemical oxidation. High-rate random telegraph noise (RTN) induced in certain oxidized devices is then observed, possibly caused by carrier trapping at or near the point defect.

Chip Design. The integrated circuit (IC) is designed in a standard 0.13-μm CMOS process (Figure 1b,c). The chip is composed of 12 low noise transimpedance amplifiers. The amplifier gain is programmable and able to handle currents ranging from hundreds of picoamperes to microamperes. The amplifier bandwidth is also tunable, providing the ability to maximize front-end bandwidth while maintaining amplifier stability.

Each amplifier is connected to 500 sensing sites distributed across five rows, resulting in 6000 total sensing sites arranged in a 60-by-100 grid. Each row can be electrically disconnected from the amplifier through programmable switches, ensuring that inactive rows do not contribute substantially to electrical parasitics. The sensing sites in any one row connect to a common measurement bus through programmable switches. Each sensing site contains two electrodes that are connected to the CNT to provide the source and drain potentials. Electrode pairs can be individually programmed to connect to one of two voltages. This allows devices to be biased at different potentials relative to the solution potential, a feature that can be utilized to control which devices undergo electrochemical reactions during functionalization. Each electrode is 15 μm × 15 μm in dimension.

Postprocessing. ICs as received from the manufacturing foundry must be extensively processed to serve as compatible substrates for the smFETs. An overview of the processing is presented below, with major processing steps and a scanning electron micrograph of a representative device highlighted in Figure 2. Additional details are provided in the Supporting Information. This processing is performed on individual chips diced from 300 mm wafers, measuring 5 mm × 5 mm.

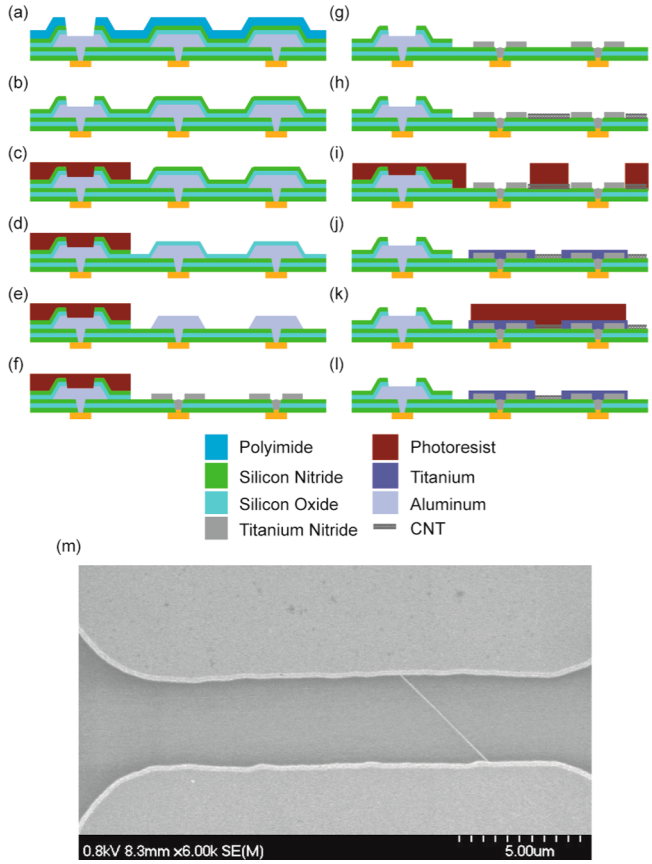

Figure 2. Postprocessing steps used to modify surface of CMOS chip depicting (a) unprocessed chip, (b) polyimide removal, (c) bond pad protection, (d) silicon nitride removal, (e) silicon oxide removal, (f) aluminum removal, (g) resist removal, (h) nanotube transfer, (i) metallization lithography, (j) contact metallization, (k) isolation lithography, (l) device isolation and photoresist removal, and (m) scanning electron micrograph of a fully processed electrode pair with single CNT bridging contacts.

A profile of the top of the IC can be seen in Figure 2, panel a. The bond pads are exposed, while the electrodes that will be used to connect to the CNTs are covered in polyimide, silicon nitride, and silicon oxide. The first postprocessing step is removal of polyimide (Figure 2b). Photodefinable polyimide is then used to protect the bond pads while exposing the electrode array for nitride removal (Figure 2c). The silicon nitride is then etched using boiling phosphoric acid (Figure 2d). Next, the silicon oxide layer is wet etched (Figure 2e). At this point, the aluminum electrodes of the array are completely exposed. The aluminum is then wet etched to reveal the

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Nano Lett. XXXX, XXX, XXX−XXX

underlying titanium nitride adhesion layer (Figure 2f). Removal of the aluminum is necessary because it is highly corrosive in electrolyte, further burdening later passivation requirements. In addition, the thin native insulating layer of aluminum oxide that forms on the aluminum pads makes contacting the CNTs difficult. Once the aluminum etch is complete, the polyimide mask is removed (Figure 2g).

With the titanium nitride electrodes exposed, CNTs can now be transferred to the surface of the chip (Figure 2h). CNTs must be transferred because the nanotube growth process requires growth temperatures in excess of 850 °C, while the CMOS substrate can only generally tolerate temperature up to approximately 350−400 °C. Popular transfer methods include solution drop casting nanotubes, which may be aided by dielectrophoresis,[12] and mechanical transfer, which is used in this study.

In our mechanical transfer approach, CNTs are grown in a CVD process using ferritin catalyst spun onto a growth substrate. A catalyst concentration of 250 ng/mL yields approximately one nanotube every 5 μm in high-density growth regions, while lower-density regions of growth consist of one nanotube every 10−20 μm. Regions of sparse growth are also observed, which impacts total yield. CNTs are generally oriented in the direction of CVD air flow, which helps ensure they are properly aligned with the electrode array during transfer. A CNT diameter distribution can be found in Figure S1. Transfer of the CNTs from the growth substrate to the IC is performed using a polycarbonate (PPC) transfer process originally developed for graphene device fabrication.[13]

After transfer of the CNTs, a metallization step is performed using titanium to bridge the connection between the transferred nanotubes and the exposed titanium nitride electrodes (Figure 2i,j). The resulting pattern leaves a 4 μm gap between the source/drain electrodes where the CNTs are exposed. To ensure that CNTs only bridge isolated electrode pairs and do not short adjacent pairs or bond pads, a CNT isolation step is performed (Figure 2k,l). Photolithography is used to protect nanotubes that bridge electrode pairs. Exposed devices not covered in photoresist are then etched with oxygen plasma.

At this point, the fully processed ICs are packaged and wirebonded in a chip carrier. Donut encapsulation is then used to protect bond wires while keeping the electrode array exposed. After encapsulation, a polypropylene reservoir is attached to the chip surface to create a test chamber of approximately 3 mL volume (see Figure S3). Additional information on test bench electronics can be found in the Supporting Information.

Prefunctionalization Device Characterization. After postprocessing is complete, integrated nanotubes are electronically characterized to determine the overall yield to this point in the fabrication process. On one representative chip, nanotubes bridge 717 electrode pairs as determined by electrical continuity tests performed in 1XPBS with a 100 mV source-drain potential applied across the devices and a −300 mV electrolytic gate bias provided by an external platinum pseudoreference electrode. Electrode pairs are scanned with a range of gain/bandwidth settings, ensuring devices of all conductance levels are discovered. The physical locations of these 717 devices can be found in Figure 3, panel a, which serves as a map of all devices detected and can aid in the analysis of the spatial distribution of transferred devices. A subset of 97 devices, drawn from a set of 495 nanotubes

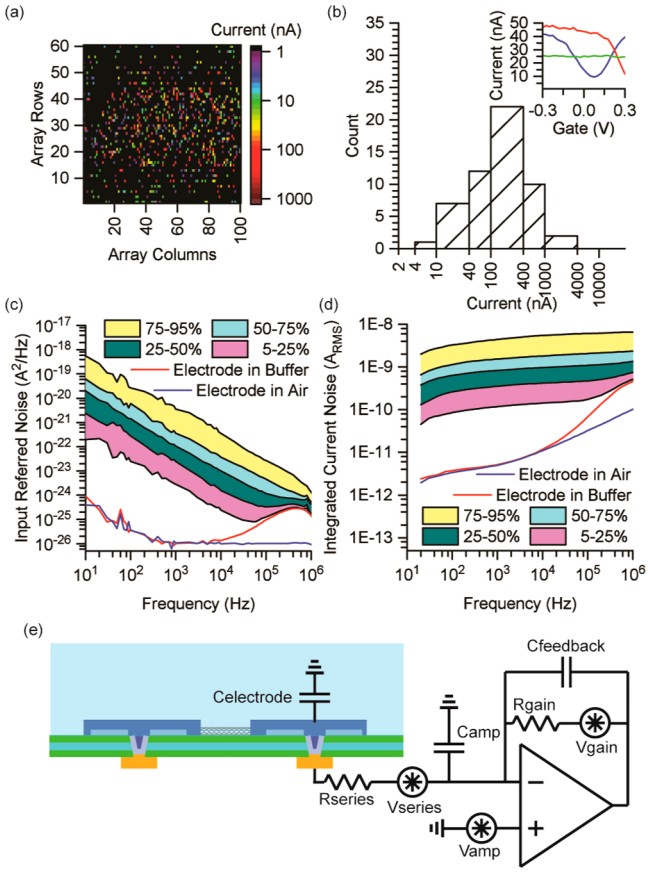

Figure 3. (a) Physical map of 717 devices detected during electrical continuity tests. (b) Histogram of the maximum current level of 54 SEM inspected devices measured in 1XPBS. Inset demonstrates current−voltage characterization of representative semiconducting and metallic devices. (c) Input-referred power spectral density of amplifier connected to an electrode in buffer, electrode in air, and of SEM inspected devices arranged in noise magnitude percentiles. (d) Integrated current noise. (e) Depiction of primary noise sources.

detected with wide-bandwidth amplifier settings, is inspected with a scanning electron microscope (SEM). Of these 97 devices, 54 devices contain only a single nanotube device, resulting in an expected yield of 399 single CNT devices on the entire chip. We find that the probability of n nanotubes spanning an electrode pair is given by a zero-inflated Poisson distribution

$$P(n) = \begin{cases} p0 + (1 - p0)e^{-\lambda} & n = 0 \\ (1 - p0)\dfrac{\lambda^n}{n!}e^{-\lambda} & n > 0 \end{cases}$$

as shown in Figure S2. This distribution is well fit by $\lambda = 1.07$ and $p0 = 0.76$. This yield can be expected to be improved further by optimizing the density and uniformity of tubes in the transfer process. Two additional chips have been fully processed, with 570 and 1127 devices discovered through electrical continuity tests.

To determine the variability in electrical characteristics of devices with one CNT connecting electrodes, current−voltage (IV) scans are performed in 1XPBS while the electrolytic gate potential is swept from −300 mV to 300 mV with respect to the source potential. Device current is monitored at a 4 MHz sample rate, and current at each gate potential is monitored for

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Nano Lett. XXXX, XXX, XXX−XXX

15−30 s, allowing noise analysis to be performed at each gate bias. A 1-MHz-cutoff fourth-order Bessel filter is used for antialiasing before data acquisition and defines the bandwidth of the system. A histogram of the maximum current level of the single CNT devices can be found in Figure 3, panel b. The inset of Figure 3, panel b demonstrates representative IV curves, with 10% of devices showing semiconducting behavior similar to the blue curve and 70% showing semiconducting behavior similar to the red curve. The remaining 20% of devices are similar to the green curve, with little response to gating consistent with metallic nanotube behavior. Both metallic and semiconducting nanotubes have been used as smFET devices though;[4,5] therefore, all devices remain candidates for biofunctionalization.

Wide bandwidth input-referred noise spectral densities of these same single-CNT devices in 1XPBS at zero gate-source bias can be found in Figure 3, panel c. The noise is fit by $S_n(f) = \frac{\alpha}{f^\beta}A^2/\text{Hz}$ where α ranges from 2.3×10^{-21}−7.6×10^{-18} with median value of 2.9×10^{-19}, and β is approximately 1.16. Nanotubes with high α exhibit a device-limited $1/f$ spectrum across the entire measurement bandwidth. Extrinsic noise begins to dominate the noise spectrum of devices with low α at frequencies greater than 100 kHz, which causes instrumentation-based degradation of the SNR of any activity beyond this frequency. Integrated current noise is depicted in Figure 3, panel d. An integrated value of 504 pA rms represents the instrumentation noise limit of the "open headstage" amplifier, that is, one connected to an electrode exposed to buffer solution.

The contributing electronic noise sources are depicted in Figure 3, panel e. Neglecting series resistance, R_{series}, the amplifier noise voltage induces a noise current across the parasitic input capacitances according to the equation

$$S_n(f) \approx (2\pi f(C_{amp} + C_{electrode})V_{amp})^2$$

Non-negligible series resistances, in the form of switch resistance, routing resistance, and electrode resistance, can also induce a noise current across the electrode capacitance. To keep high frequency noise to a minimum, electrode capacitance $C_{electrode}$ should be kept as small as possible. This can be achieved by minimizing the surface area of the contact electrode. The ability to connect vertically to electrodes in CMOS substrates allows the electrode area to be reduced in our case to less than 300 μm^2, resulting in $C_{electrode}$ of approximately 34 pF. $C_{electrode}$ could be reduced further with passivation of the electrodes that contact the nanotubes. The higher parasitic $C_{electrode}$ values characteristic of nonintegrated smFET devices, in particular those with large nonpassivated electrodes, can lead to instrumentation noise dominating nanotube noise over a much wider range of α and at much lower frequencies. Cointegration of smFET devices with low-noise amplifiers in CMOS substrates also eliminates parasitic capacitances associated with cabling and PCB traces, providing further advantages over nonintegrated platforms.

In addition to limiting effective bandwidth through SNR, large parasitic capacitances can also result in attenuation of the sensor frequency response. $C_{electrode}$ creates a low-pass filter with any resistances in series between the electrode and the measurement amplifier. With $C_{electrode}$ of 34 pF and approximately 1.2 kΩ of resistance due to the switch matrix, the front-end bandwidth extends to 4 MHz.

Electrochemical Functionalization. Electrochemical functionalization is performed in 0.5 M sulfuric acid. The solution potential is lowered relative to the nanotube using the external platinum electrode, while the nanotube current is continuously monitored. When the solution potential reaches the oxidation threshold, a large current drop is observed. The current drop indicates that a reaction has occurred on the CNT sidewall, producing an oxidative defect that creates the charge-sensitive conduction barrier. Subsequently, the solution potential is increased to stop further oxidation. A partial and complete oxidation of two devices can be seen in Figure 4,

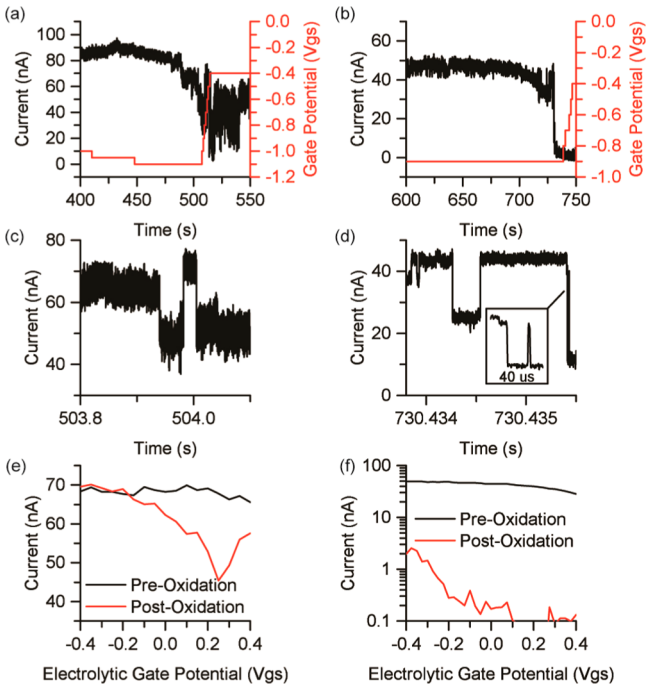

Figure 4. (a) Partial and (b) complete electrochemical oxidation of two devices in 0.5 M sulfuric acid. Major oxidation event of (c) partially oxidized and (d) completely oxidized devices. Current−voltage curves before and after (e) partial and (f) complete oxidation.

panels a and b, respectively, with the major oxidation event of each device highlighted in Figure 4, panels c and d, and before-and-after oxidation IV curves recorded in saline solution provided in Figure 4, panels e and f.

Closer examination of the oxidation events highlighted in Figure 4, panel d reveals a rich level of activity now evident because of the bandwidth with which this measurement can now be performed, providing additional insight into the electrochemical reaction. During oxidation, only a few dominant events had a substantial impact on conductance levels. During some of these events, the device current rapidly transitions through very short-lived intermediate steps, some of which had lifetimes of no more than a few microseconds. The close temporal proximity of these intermediates to the large conductance drops suggests that the events may be strongly correlated and may indicate additional reaction pathways with unique scattering signatures only resolvable at high bandwidth.

Random Telegraph Noise. Two devices that underwent electrochemical oxidation exhibited high-rate RTN fluctuations after functionalization, providing an opportunity to study fast events in these smFET devices without biomolecular attachment. Such spontaneous RTN behavior is an additional yield issue for smFET devices; study of this effect is important also to reducing this yield detractor.

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Nano Lett. XXXX, XXX, XXX−XXX

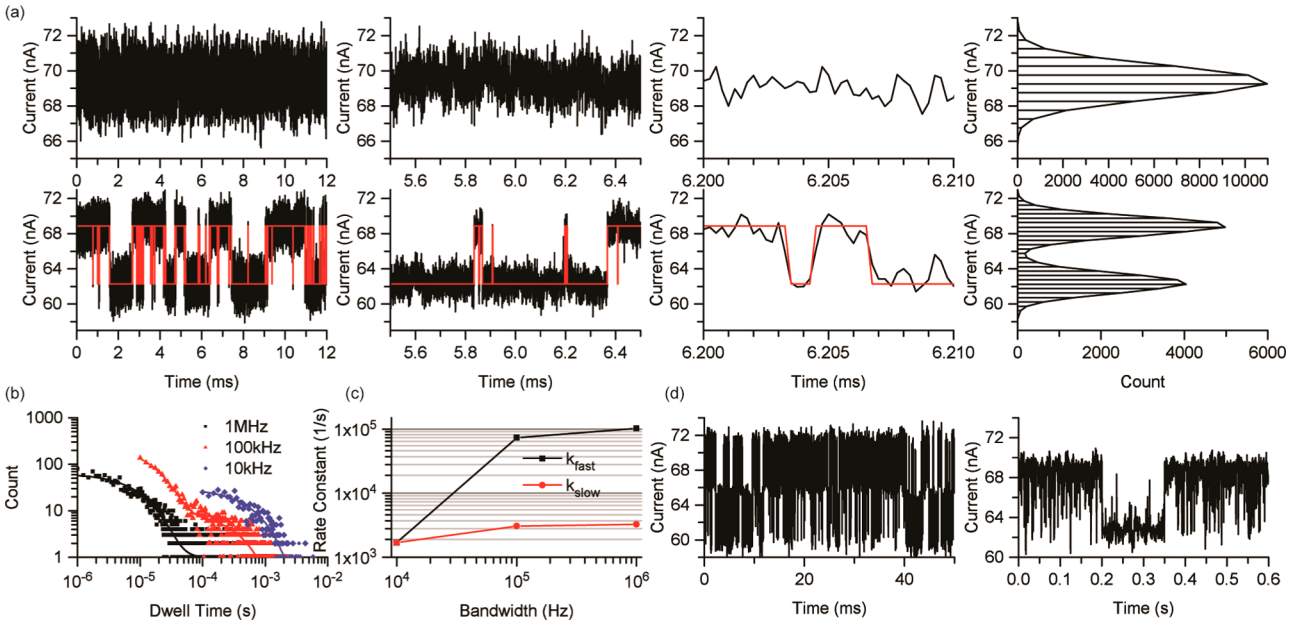

Figure 5. (a) Device current recorded at 4 MHz sample rate. Top row: Device current before electrochemical oxidation. Bottom row: RTN recorded after oxidation with idealized two state behavior shown in red. First column: Representative recording over 12 ms window. Second column: Data over a 1 ms window within the 12 ms-window trace. Third column: Data over a 10 μs window within the 1 ms-window trace. Fourth column: Histogram of device current. (b) High conductance state dwell time histograms for 1 MHz, 100 kHz, and 10 kHz bandwidths. (c) Extracted kinetic rate constants as a function of measurement bandwidth. (d) Dynamic disorder in oxidized device recorded over two different measurement time scales.

Before-and-after-oxidative-functionalization time-series plots at various time scales of a partially oxidized device are shown in Figure 5, panel a. Idealized traces are plotted in red and are used for kinetic analysis. Idealization is performed by automated baseline drift removal[14] followed by HMM analysis with the vbFRET software package.[15] Performing idealization using wavelet denoising and thresholding yields comparable results. A histogram of raw-data current levels before and after oxidation can be seen in Figure 5, panel a as well and illustrates a SNR of 4.3. A dwell time histogram of the idealized data is plotted in Figure 5, panel b. Hundreds of dwells on order of 1 μs in duration are extracted, further illustrating the temporal resolution of this test platform. RTN rate constants are extracted from double exponential fits to the dwell time histogram according to the equation

$$P = Ae^{-k_{\text{fast}}t} + Be^{-k_{\text{slow}}t}$$

as can be seen in Figure 5, panel c. In addition to extracting values for the 1 MHz bandwidth (4 MHz sample rate) used during data acquisition, the transient data is filtered and downsampled to effective bandwidths of 100 kHz (sampled at 400 kHz) and 10 kHz (sampled at 40 kHz) to illustrate the error associated with capturing fast data at insufficient bandwidth. Significant error is observed, for example, in the extraction of the fastest rates and reduced bandwidths. At 10 kHz, the fast exponential term is no longer apparent, and data is fit to a single exponential. The key metric here is the ratio of the measurement bandwidth to the extracted rate constant. High values of this ratio are important to ensure missed events do not severely alter the extracted rate values.[16]

Metastability in conductance levels has been observed during electrochemical oxidation of carbon nanotubes in other work and was attributed to the breaking and reforming of a covalent bond with a bisulfate ion on the CNT sidewall.[17] We also observe this metastability during oxidation in sulfuric acid, but the existence of RTN during postoxidation recordings in saline solution suggests the RTN we observe may have an alternative source.

RTN in nonfunctionalized nanotubes has largely been attributed to charge traps in close proximity to the CNT.[18−24] RTN has also been attributed to charge trapping induced modulation of a barrier in nanotube film Schottky junctions,[25] in nickel silicide Schottky contacts,[26] and in the base-emitter junction of SiGe transistors.[27] One explanation for the RTN observed after oxidation could be the existence of a charge trap in the vicinity of the charge-sensitive defect site. Before oxidation, the trap contributes to the flicker noise spectrum that dominates nanotube noise current. The low conductance state observed after oxidation may be attributed to scattering from a defect-induced conduction barrier, while the barrier seems relatively transparent to carriers in the high conductance state. Shifts in the barrier height due to the charge trap may be the cause of the RTN fluctuations. Alternatively, localized energy states are thought to sometimes be created in point defected nanotubes,[28] which might serve as traps that could induce RTN in the device. Electrochemical oxidation studies of suspended nanotubes would help assess this explanation by removing the possibility of substrate-induced trapping.

One additional characteristic of the RTN observed in this study is dynamic disorder, resulting in periods of fluctuating kinetics, which necessitates the use of a double exponential model for dwell time fits. Temporal examples can be seen in Figure 5, panel d. Under the same bias conditions, the RTN fluctuates between high rate activity and low rate activity. Carrier capture time for a charge trap follows the equation $\tau_c = 1/n\nu\sigma$, where n is the carrier density per unit volume, ν is the carrier thermal velocity, and σ is the capture cross-section. The

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Nano Lett. XXXX, XXX, XXX−XXX

thermal velocity of a carrier changes as the square root of temperature changes and is unlikely to modulate enough to cause the change in rate constants observed. The dynamic disorder may be related to fluctuations in the capture cross-section area or a change in local carrier concentration due to interactions between the electrolyte and the defect region.

Conclusion. The integrated smFET platform has been demonstrated through electrolytically controlled device characterization and electrochemical oxidation. The detection of high-rate RTN further illustrates the temporal resolution of the measurement system. Future work will complete the biofunctionalization of oxidized devices by tethering probe biomolecules to the defect site to enable high bandwidth biomolecular studies.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.nanolett.6b00319.

Additional information on CMOS chip postprocessing, CNT growth diameter distribution, device count probability, experimental setup, and test bench (PDF)

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Notes

The authors declare no competing financial interest.

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