28.5 1.1 to 1.6GHz Distributed Differential Oscillator Global Clock Network

Steven C. Chan[1], Kenneth L. Shepard[1], Phillip J. Restle[2]

[1]Columbia University, New York, NY
[2]IBM, Yorktown Heights, NY

Distributing a low skew, low jitter, and low power global clock in the presence of PVT variations is a significant challenge. Increasing clock latency relative to cycle time has resulted in more skew and jitter due to mismatches (PVT) in the global clock distribution. Recent work has demonstrated that resonating the clock capacitance with an inductance can result in better phase stability (skew and jitter) and power savings [1-3]. In this work, a distributed differential oscillator global clock network using on-chip spiral inductors is designed. This clock network is uniform in both amplitude and phase across the distribution, unlike [2] and [3], respectively, and does not require, as in [1], a buffered clock tree to distribute the drive or the addition of large decoupling capacitors. In addition, unlike the single-ended distribution of [1], in this work, differential detection of the global clock in the local clock buffers results in reduced jitter due to power-supply noise and other common-mode noise sources [4], despite the slower signal slew rates characteristic of the more sinusoidal clocks resulting from resonance.

Figure 28.5.1 shows the proposed global clock distribution. Four spiral inductors are placed symmetrically around the global clock network and "H-treelets" are used to route the clock from the inductors to the global clock grid. The treelets distribute the drive of the inductors thereby improving skew. Four negative differential transconductors are used to compensate for loss and maintain oscillation, with the bias current, I_{bias}, determining the clock amplitude. Up to 5pF can be added to ϕ and $\overline{\phi}$ through switchable MOS capacitors, C_{tune}, to provide tuning of the oscillation frequency from 1.6 to 1.1GHz. A small variable-strength buffer positioned at the center of the clock network provides injection locking to a reference.

The design is fabricated in a 0.18μm 1.8V mixed-signal CMOS technology with 6 levels of aluminum wiring. The distribution, shown approximately to scale in Fig. 28.5.1, is 2mm × 2mm. Both ϕ and $\overline{\phi}$ have a capacitive load of 13pF; 9pF is from the clock wires themselves while the remainder is from local clock buffering and on-chip test and measurement circuitry. No shielding of the clock grid wires is necessary, since ϕ and $\overline{\phi}$ provide return paths for each other (0.4nH/mm). The 6nH differentially driven symmetric spiral inductors have a diameter of 280μm and are stacked on M6 and M5 to reduce series resistance. It is straightforward to replicate and tile the network in Fig. 28.5.1 to create a much larger global clock distribution. Scaling to at least 10GHz is possible by simply reducing the size of the inductors. Figure 28.5.2 shows a die micrograph. A differential non-resonant global clock network driven by a conventional clock H-tree and a clock grid is also designed on the same test chip for comparison.

Figure 28.5.3 shows the magnitude of the differential driving point admittance as a function of frequency as measured by probing the center of the resonant and non-resonant clock grids with zero common-mode bias using GSG probes. For the resonant network, C_{tune} is swept from 0 to 5pF in steps of 1.65pF, with lowest tank Q at the largest value of C_{tune}. The resonant frequency varies by at most 4% as the common-mode bias on the clock is swept from 0 to 1.8V for C_{tune} = 0pF since the linear wire capacitance dominates. When C_{tune} = 5pF, non-linear gate capacitance is almost half the total tank capacitance and the resonant frequency varies by up to 9% with bias.

Figure 28.5.4 shows the envelope of the resonant clock oscillations (the high and low voltage levels of the clock) as measured using a high-impedance active probe. The envelope voltage is plotted versus I_{bias} for C_{tune} = 0 and 5pF. The minimum I_{bias} for start-up is 0.06mA and 0.13mA for C_{tune} = 0 and 5pF, respectively. At these biases, the clock amplitude is only 140mV. At around 1mA, the clock is approximately full-rail for both cases. There is more overshoot and undershoot in the clock waveforms for C_{tune} = 0pF because of the higher tank Q.

Figure 28.5.5 shows peak and rms cycle-to-cycle jitter as measured using an open-drain buffer after conversion to a full-rail single-ended clock with the local clock buffer shown in Fig. 28.5.6 [5]. Jitter in the resonant clock network is plotted as a function of I_{bias} for no added power supply noise and 300mV of added power supply noise. At low I_{bias}, the clock is susceptible to supply-noise induced jitter due to reduced signal swing. Jitter is minimized by setting I_{bias} to be just large enough to ensure close to full-rail oscillations. Larger values of I_{bias} degrade jitter, because the current source device in the negative transconductor becomes triode, allowing power-supply noise to couple into the clock network. A bias current of 0.8mA minimizes jitter (peak = 22ps, rms = 3.2ps for no added supply noise; peak = 36ps, rms = 6.6ps for 300mV of added supply noise) for C_{tune} = 0pF at 1.6GHz. The non-resonant differential global clock network is measured to have 65ps and 9.6ps of peak and rms jitter, respectively, at 1.0GHz, the target operating frequency, with no added supply noise. With 300mV of added supply noise, the peak and rms jitter are measured to be 201ps and 58.9ps, respectively, almost an order of magnitude larger than the jitter in the resonant clock.

An average DC current of 26mA is drawn from the supply of the resonant clock network for C_{tune} = 0pF at 1.6GHz with I_{bias} = 0.8mA, while the non-resonant clock network draws 70mA at 1.0GHz. There is almost 50% less load capacitance in the non-resonant clock network than in the resonant clock network (7pF versus 13pF), yet the non-resonant scheme consumes almost three times as much power at 1.0GHz as the resonant scheme at 1.6GHz.

A distributed differential oscillator global clock network using on-chip spiral inductors is presented. The clock distribution has low latency and strong immunity to power-supply-noise-induced jitter. It achieves almost an order of magnitude less jitter than a conventional differential non-resonant tree-driven-grid global clock distribution and uses almost 3-times less power.

Acknowledgements:
This work was supported in part by the MACRO C2S2 Focus Center under contract 2003-CT-888, the SRC, and the NSF under contract CCR-00-86007.

References:
[1] S. C. Chan et al., "A 4.6GHz Resonant Global Clock Distribution Network," *ISSCC Dig. Tech. Papers*, pp. 342-343, Feb., 2004.
[2] F. O'Mahony et al., "10GHz Clock Distribution Using Coupled Standing-Wave Oscillators," *ISSCC Dig. Tech. Papers*, pp. 428-429, Feb., 2003.
[3] J. Wood et al., "Multi-GigaHertz Low-Power Low-Skew Rotary Clock Scheme," *ISSCC Dig. Tech. Papers*, pp. 400-401, Feb., 2001.
[4] F. E. Anderson et al., "The Core Clock System on the Next Generation Itanium Microprocessor," *ISSCC Dig. Tech. Papers*, pp. 146-147, Feb., 2002.
[5] J. G. Maneatis, "Low-Jitter Process-Independent DLL and PLL Based on Self-Bias Techniques," *IEEE J. Solid-State Circuits*, vol. 31, no. 11, pp. 1723-1732, Nov., 1996.

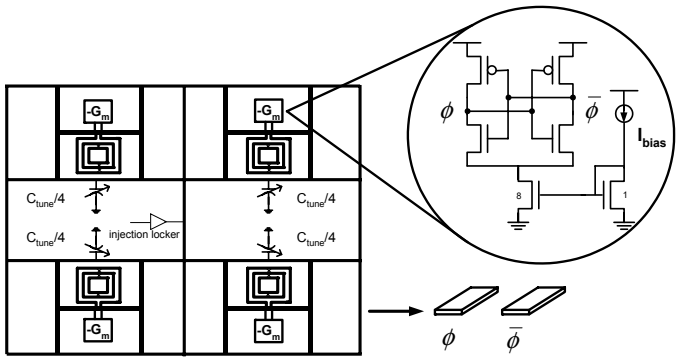

Figure 28.5.1: A distributed differential oscillator global clock network.

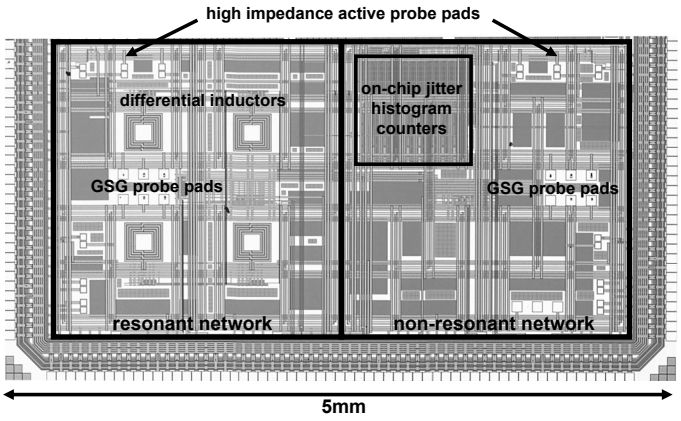

Figure 28.5.2: Die micrograph.

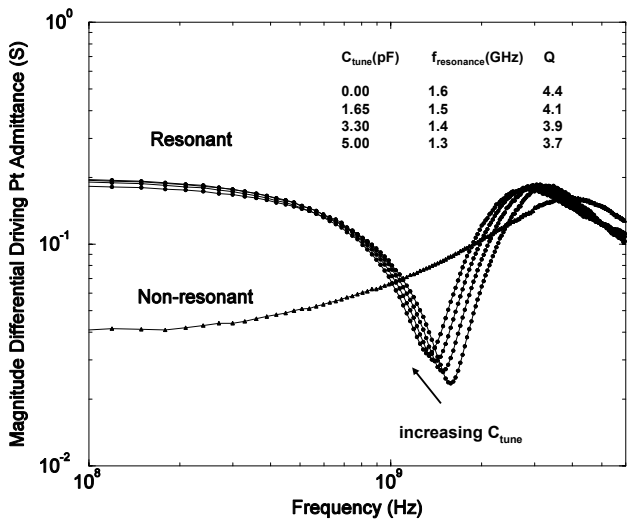

Figure 28.5.3: Differential driving point admittance.

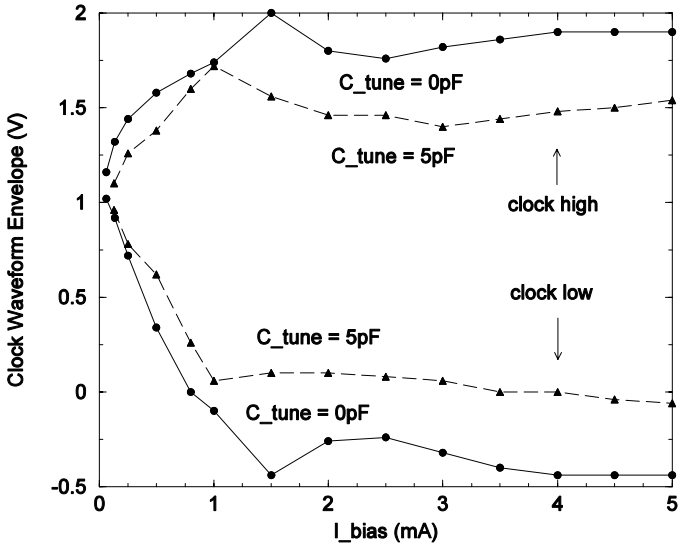

Figure 28.5.4: Resonant clock waveform oscillation envelope.

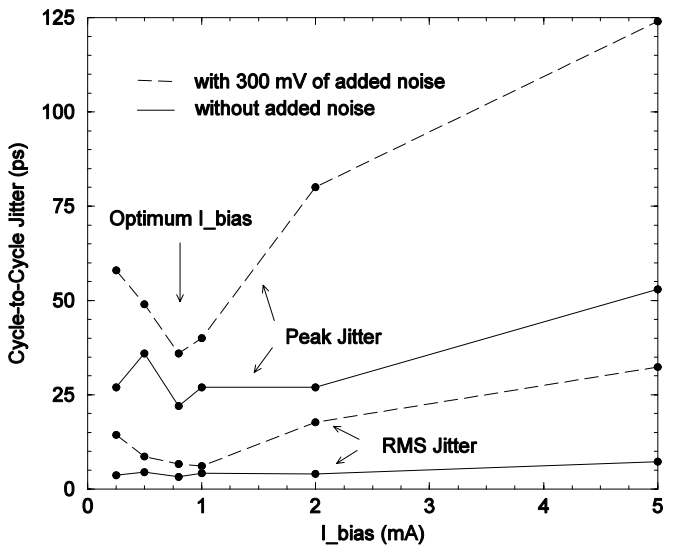

Figure 28.5.5: Resonant clock jitter with and without added supply noise.

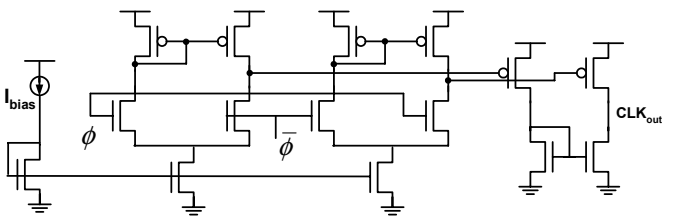

Figure 28.5.6: Local clock buffer.

28