16.4 High-Tension Power Delivery: Operating 0.18μm CMOS Digital Logic at 5.4V

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Operating at supply voltages below 1V, 90nm (and below) technologies still demand in excess of 100W of power in the largest chips. Delivering this power at the reduced supply voltage levels required by technology scaling results in high-current requirements, exacerbating electromigration concerns and power-supply integrity issues (i.e., forcing very low impedance requirements on the power distribution). Being able to bring the power onto the chip at higher voltage levels (high-tension lines), and then down-converting to the required supply voltage, significantly reduces the off-chip current requirements.

DC-DC downconversion with switching regulators[1] can achieve high energy efficiency, but it requires off-chip inductors. In this paper, high energy efficiency is realized with an *implicit* on-chip DC-DC conversion [2] approach that "stacks" logic, two or three high, and operates the entire stack at a multiple n of the supply voltage, nV_{DD}, as shown in Fig. 16.4.1. By stacking the logic domains n high, the current demands on the power and ground networks are also reduced by a factor of n over the current demands of all of the domains running in parallel at V_{DD}. As shown in Fig. 16.4.1, active regulation in the form of linear regulators is required on the "internal" supply nodes to compensate for transient and steady-state charge imbalance. In addition, level-shifting circuits are required to interface logic between the domains. Both the level-shifting circuits and regulators operate over a greater-than-V_{DD} supply range. Despite this, thin-oxide devices in a triple-well 0.18μm process are used throughout, with startup circuits to ensure that these devices are not overstressed during power-on. Only well-substrate junctions that have breakdown voltages of more than –15V, are subject to potentials in excess of V_{DD}.

Interfacing between domains is provided by the level-shifting circuits shown in Fig. 16.4.2. The n-to-m shifters convert a logic level between nV_{DD} and $(n-1)V_{DD}$ (denoted n-logic in Fig. 16.4.1) to one between mV_{DD} and $(m-1)V_{DD}$. The inverters denoted with the number n are operating with n-logic signals. In the 1-to-2 shifter, the level shifting is provided by the NMOS-PMOS stack with gates tied at V_{DD}. Capacitors M1 and M2 improve the latency of the level-shifter by more quickly establishing the differential voltage required to switch the output cross-coupled inverter pair. The topology for the 2-to-1 shifter is similar. In this case, however, overstress of the M1 and M2 capacitors is possible during start-up as the external supply is powered on; devices M3 and M4, on during start-up, are added to prevent this possible overstress. The 1-to-3 level shifter is implemented by cascading a 1-to-2 and a 2-to-3 level shifter. A single-stage topology (Fig. 16.4.2) is also possible but is found to be slower than the multi-level implementation and does not allow for a "bootstrap" capacitor implemented as a thin-oxide transistor.

Figure 16.4.3 shows the details of the push-pull linear regulators that are used to establish the intermediate voltage levels (and how they are configured for the case of $3V_{DD}$ downconversion). These regulators add or subtract charge as required when the stacked domains are mismatched in their charge consumption. To achieve fast response time for the regulator and thereby reduce the decoupling capacitance requirements, replica biasing is used to bias the output-state drivers [3]. These drivers have their own feedback loops (labeled 3 and 4) to rapidly respond to output current transients. In normal operation, when current is sourced (sunk) from V_{out}, M3 (M4) is almost off and transistor M1 (M2) handles nearly all of the load current. The DC output impedance of these drivers is less than 4.5Ω. The regulator along with explicit decoupling capacitance of C_{decap}= 50pF guarantees a droop (ΔVout) of less than 180mV for I_{max} = 40mA, leading to a response time of $C_{decap}\Delta V_{out}/I_{max}$ = 225ps. The feedback loops labeled 1 and 2, have bandwidths of 40MHz with a phase margin of 80^0. Capacitors C_1=C_2=4pF quiet coupling noise from the (large) gate-to-source capacitances of transistors M3 and M4. The regulator consumes a quiescent current of 4mA, leading to a 90% current efficiency at I_{max}. Although none of the devices are overstressed during steady-state operation of the regulators, the power transistors can be overstressed during start up. Currently, the start-up voltage, $V_{startup}$ is brought in from off-chip to appropriately condition V_{out} through a forward-biased diode to prevent overstress. Once the system is powered up, $V_{startup}$ is reduced to zero and the diode is reverse biased. A similarly simple startup scheme is employed for nodes internal to the error amplifiers.

To verify the application of this approach to "standard" digital logic and design methodologies, both the $2V_{DD}$ and $3V_{DD}$ down-conversions of Fig. 16.4.1 are implemented on a single chip. Figure 16.4.7 shows a micrograph of the chip. Each logic domain is a 16×16 pipelined fixed-point multiplier designed to operate at 650MHz, synthesized into a digital standard-cell library in a TSMC 0.18μm technology with V_{DD} = 1.8V. The relative activity of the domains can be controlled by zeroing out leading-order bits of the multiplier and multiplicand being input to a given domain. In Fig. 16.4.4, the measured energy efficiency is shown as a function of relative activity between the domains; the numbers denote the number of "zeroed" bits in each domain (e. g., for the $3V_{DD}$ system, 0-2-0 indicates that the leading 2b of the multiplier and multiplicand input to the middle domain are zeroed). Peak energy efficiency of almost 93% is achieved for the 0-0 case in the $2V_{DD}$ system at 650MHz. Results for the $3V_{DD}$ system are only shown at 300MHz operating frequency because of an unintended long path in the design. Energy efficiencies greater than 80% are achieved despite the low current efficiency at this operating frequency.

The chip incorporates an on-chip 40MHz 8b Flash ADC to monitor the regulation of the *internal* V_{DD} and $2V_{DD}$ nodes. Figure 16.4.5 shows the outputs of these power-supply-monitoring ADCs, showing better than 10% regulation for the multipliers running with random input patterns. Figure 16.4.6 shows the transient operation of the 1-to-2 level-shifting circuits transforming a 400MHz 1-logic clock input, obtained by picoprobing.

An approach for "stacking" logic to achieve *implicit* on-chip DC-DC conversions with greater than 90% energy efficiency and little area overhead has been presented.

Acknowledgements:
This work was supported in part by the MARCO, C2S2 Focus Center (contract 2003-CT-888), the SRC and the NSF (contract CCR-00-86007).

References:
[1] G.-Y. Wei and M. Horowitz, "A Fully Digital, Energy-Efficient Adaptive Power-Supply Regulator," *IEEE J. Solid-State Circuits*, vol. 35, pp. 520-528, April, 2000.
[2] S. Rajapandian and K. L. Shepard, "Energy-Efficient Low-Voltage Operation of Digital CMOS Circuits Through Charge-Recycling," *Symp. VLSI Circuits*, pp. 330-333, June, 2004.
[3] P. Hazucha et al., "An Area-Efficient, Integrated, Linear Regulator with Ultra-Fast Load Regulation," *Symp. VLSI Circuits*, pp. 218-221, June, 2004.

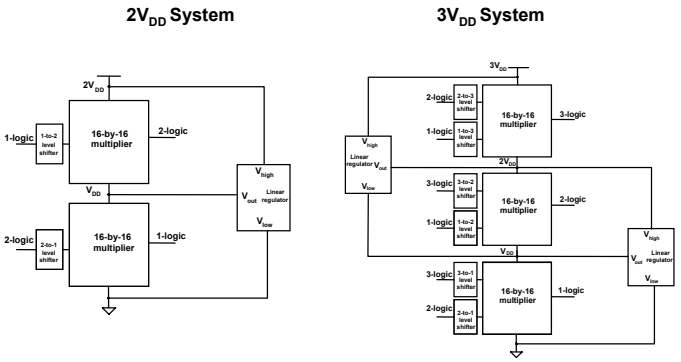

Figure 16.4.1: High-tension power delivery through implicit voltage conversion

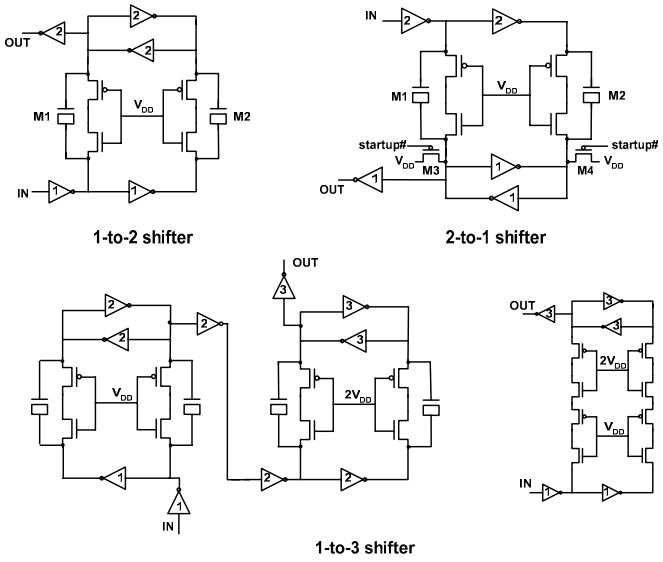

Figure 16.4.2: Level-shifting circuits

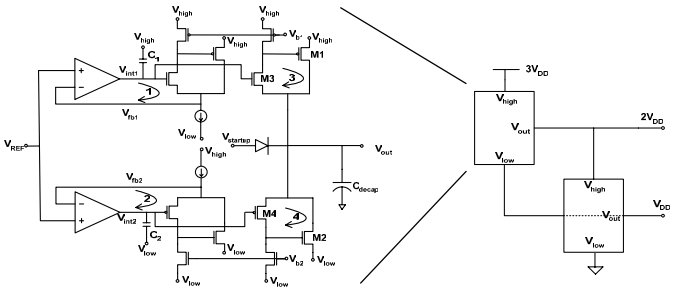

Figure 16.4.3: High-speed regulators used to regulate the VDD and 2VDD internal supply nodes

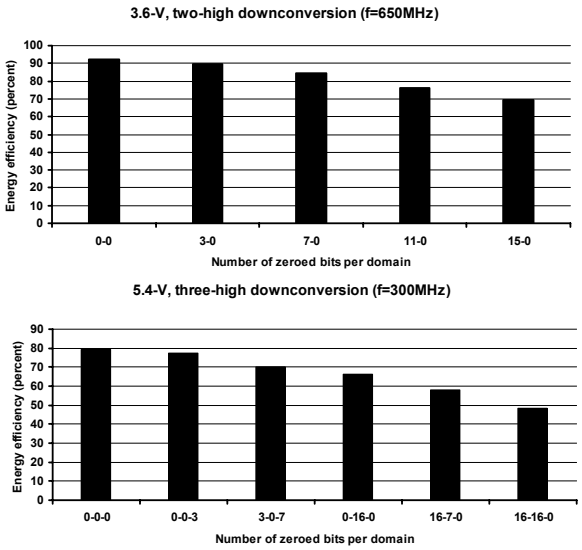

Figure 16.4.4: Energy efficiency for both 3.6V and 5.4V downconversion

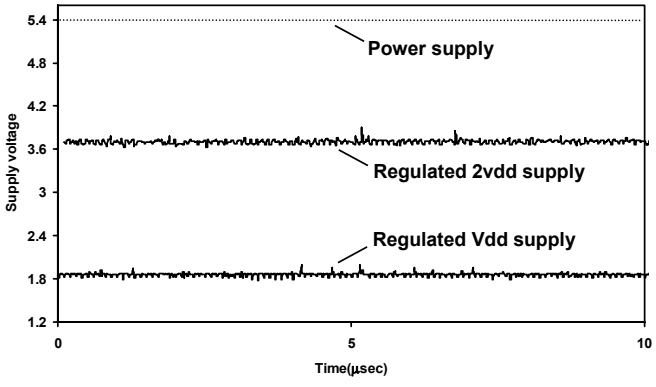

Figure 16.4.5: On-chip supply regulation as measured by the two on-chip flash ADCs

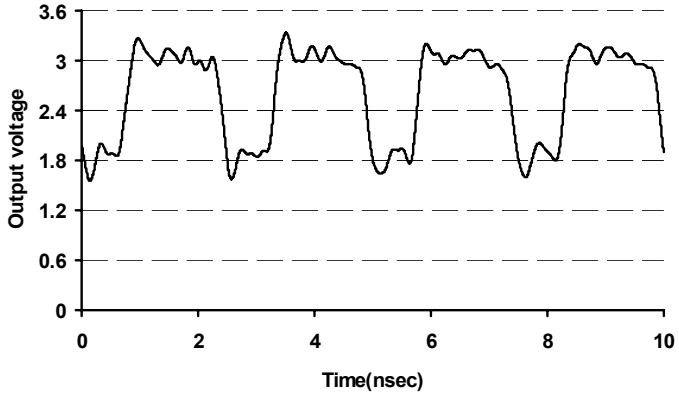

Figure 16.4.6: Level-shifted 400MHz clock at the output of a 1-to-2 level shifter

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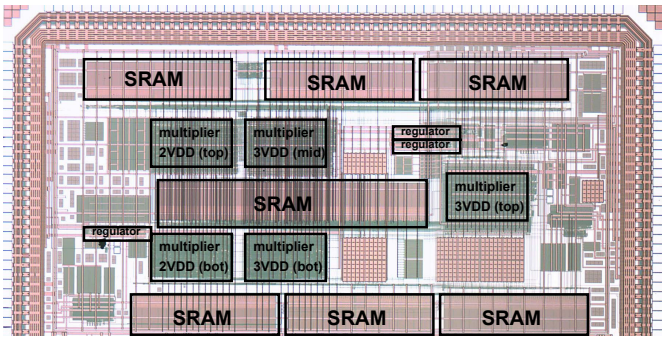

Figure 16.4.7: Die micrograph.

