Figure 4: AOI fitting results for V_H noise on input D: (a) percentage error of the fit for each case; and (b) peak sensitivity value for each case.

Figure 5: Accuracy of the fit for the entire $S(t)$ curve for two cases corresponding to V_L noise sensitivity on input D: (a) "typical" case; and (b) the case corresponding to the worst percentage error in the peak sensitivity.

on input D. Figure 4(b) shows the corresponding sensitivity values for each of these cases.

It is interesting to note that although the parameters in Table 1 can be regarded as fitting parameters, they do retain physical meaning. The nFET and pFET devices are sized for equivalent drive; therefore, all the β values are comparable. The V_T values match closely the device threshold voltage. C_{int} values show variation due to "Miller" amplification of device feedback capacitances. The fundamental reason why simple (and yet very accurate) models are possible for noise (as distinct from timing) is that voltages are always "near" the rails so that accuracy over a large voltage range is not required.

The appreciate the accuracy of the model in fitting the entire $S(t)$ curve, we look at two curves (for two different cases) associated with V_L noise sensitivity on input D. In Figure 5(a), we consider a "typical" case with $< 2\%$ error in the peak sensitivity, while in Figure 5(b), we consider the case corresponding the worst percentage error in the peak sensitivity (14.6 %). The "typical" agreement is excellent; even the worst-case seems tolerable.

4 Conclusions and future work

We have presented a very simple model that allows the characterization of standard cells for noise stability. This brings more accurate ac noise margins to static noise analysis tools examining the effects of coupling noise on functionality for standard-cell ASICs. Future work involves extending this modelling approach to handle the more complex case of pass-gate channels on the inputs or outputs. This case is generally avoided in standard-cell libraries because of noise considerations and timing modelling difficulties. Pass-gate channels will have to be modelled by nonlinear conductances, which adds considerable complexity fo the model (and many more additional parameters), defying simple analytic evaluation. For nFETs passing V_L noise or pFETs
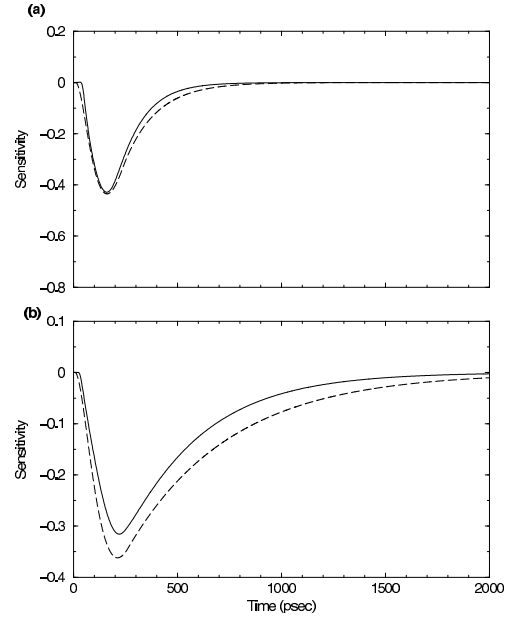
passing V_H noise, the FETs are trioded and can be modelled by a constant conductance. For nFETs passing V_H noise or pFETs passing V_L noise, the FETs go from cut-off to trioded operation and must be modelled with a conductance dependent on noise magnitude.

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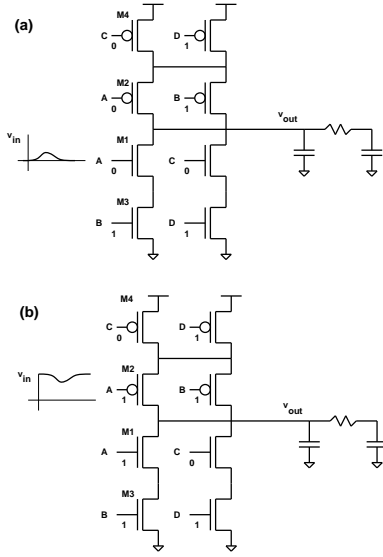
Figure 3: Simplified model for noise stability that applies to most complementary static CMOS gates.

The noise sensitivity model proposed here applies a set of four parameters $(V_T, \beta, G_r,$ and $C_{int})$ to each cell input for each noise type to which the gate is sensitive. For cells for which this modelling is valid, only V_L and V_H noise sensitivity is possible. These parameters allow standard cell inputs to be modelled by the circuit of Figure 2. The transistors trying to hold $\tilde{v}_{out}$ quiet are trioded (and are hence approximated by a linear conductance G_r) while the transistor (or in some cases transistors) being acted upon by the input noise at its gate is modelled by the current source, driven into saturation from cut-off when the noise exceeds the threshold voltage. The current source models this action as a square-law saturated current-voltage (IV) characteristic. The physical basis for this model ignores subthreshold conduction for input voltages below V_T and also assumes that velocity saturation effects are not significant. However, since both β and V_T, like the other parameters (G_r and C_{int}), are ultimately treated as fitting parameters in the model, they can adjust somewhat to compensate for inaccuracies in the model introduced by these assumptions. We note that the current source is the only circuit element that provides gain in the model and is, therefore, responsible for producing any noise instabilities. C_{int} represents the self-loading of the gate at its output. In the case that the standard cell contains only a single CCC between input and output, so that the load of the gate influences the noise stability, we use a "pi-model" to represent the (potentially resistively-shielded) external load.

Analytic solution for the sensitivity $S(t)$ is possible for the model of Figure 2 using the time-domain abstraction of Equation 1. We first recognize that the direct sensitivity circuit with respect to V_{dc} is identical to the circuit of Figure 2 except that the current source is now given by:

$$2\beta(V_{dc} - V_T + ke^{-p_1 t} - ke^{-p_2 t}) \left[u(t - t_0) - u(t - t_0') \right]$$

where t_0 and t_0' are given by the times at which $\tilde{v}_{in}$ just equals V_T, the points of activation and deactivation of the current source. Solving the sensitivity circuit for $S(t) =$

Input	Type	V_T (V)	G_r (mS)	β mA/V^2	C_{int} fF	Max % error	Avg % error
D	V_H	0.459	0.286	0.129	18.2	15.8	2.10
D	V_L	0.391	0.265	0.205	31.1	14.6	1.92
C	V_H	0.477	0.281	0.131	15.0	17.5	2.12
C	V_L	0.300	0.241	0.125	33.5	19.2	2.55
B	V_H	0.362	0.389	0.107	9.80	10.8	1.39
B	V_L	0.407	0.257	0.208	15.1	14.4	1.96
A	V_H	0.387	0.369	0.109	8.74	11.2	1.73
A	V_L	0.300	0.226	0.118	13.1	15.8	2.62

Table 1: Results of the fit for the static AOI gate.

$\partial \tilde{v}_{out}/\partial v_{dc}$ gives:

$$S(t) = \tilde{S}(t, t_0) - \tilde{S}(t, t_0')$$

where

$$\tilde{S}(t, t_0) = u(t - t_0) \left\{ -2\beta(V_{dc} - V_T)/G_r \right.$$
$$- \frac{2k\beta(1 - p_1 C_{far}R)e^{-p_1 t}}{G_r - p_1 C_{far}RG_r + p_1^2(C_{near} + C_{int})C_{far}R - p_1(C_{near} + C_{int}) - p_1 C_{far}}$$
$$+ \frac{2k\beta(1 - p_2 C_{far}R)e^{-p_2 t}}{G_r - p_2 C_{far}RG_r + p_2^2(C_{near} + C_{int})C_{far}R - p_2(C_{near} + C_{int}) - p_2 C_{far}}$$
$$- \frac{1 - r_1 C_{far}R}{(C_{near} + C_{int})C_{far}R(r_2 - r_1)} \left[\frac{2\beta(V_{dc} - V_T)}{r_1} + \frac{2k\beta}{p_1 - r_1}e^{-p_1 t_0} \right.$$
$$\left. - \frac{2k\beta}{p_2 - r_1}e^{-p_2 t_0} \right] e^{-(t - t_0)/r_1}$$
$$+ \frac{1 - r_2 C_{far}R}{(C_{near} + C_{int})C_{far}R(r_2 - r_1)} \left[\frac{2\beta(V_{dc} - V_T)}{r_2} + \frac{2k\beta}{p_1 - r_2}e^{-p_1 t_0} \right.$$
$$\left. - \frac{2k\beta}{p_2 - r_2}e^{-p_2 t_0} \right] e^{-(t - t_0)/r_2}$$

r_1 and r_2 are the roots of

$$s^2 C_{near}C_{far}R + s(C_1 + C_2 + C_2 RG_r) + G_r = 0$$

3 Regression of an AOI gate

We have used this model to generate rules for a typical standard-cell library. To further understand the utility of this model to typical standard-cell circuits, we consider details of the regression of the complementary static AOI gate shown in Figure 3. We consider the sensitivity of input A, but the other inputs follow similarly. Figure 3(a) shows how the inputs are held to provide the worst-case sensitivity to V_L noise at input A. G_r models the effective conductance of the pFET devices $M2$ and $M4$ holding $v_{out} = v_2$ high. The current source models the FET $M1$ being turned on by the action of the noise on v_{in}. Figure 3(b) shows the sensitization producing the worst-case V_H noise on A. G_r in this case models the effective conductance of the NMOS devices $M1$ and $M3$ holding v_{out} low, while the current source models the action of transistor $M2$.

Using the analytic sensitivity equation, we fit the peak noise sensitivity as determined by circuit simulation with our model of Figure 2. (Our circuit simulation engine natively supports sensitivity calculation.) This fitting involves 250 cases for each input and each noise type. These cases span a wide range of possible input waveforms (different V_{dc}, k, p_1, and p_2 values) and output loads (different C_{near}, C_{far}, and R values) carefully chosen to produce peak sensitivity in the "sweet spot" for characterization between 0.1 and 0.6. The results for the AOI gate are shown in Table 1. In all cases, the average error of the fit (as determined by the peak sensitivity) is on the order of 2 % and the worst-case error is on the order of 15 %. Figure 4(a) shows the percentage error associated with each of the 250 cases for V_H noise sensitivity
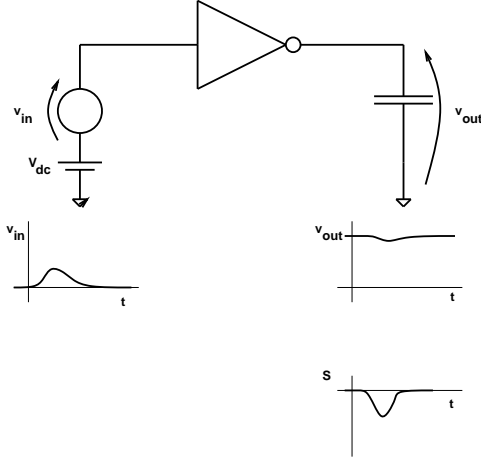
Figure 1: Calculating the dc-noise sensitivity for a CMOS inverter. $v_{in}(t)$ on the input propagates to $v_{out}(t)$ on the output. The dc-noise sensitivity $S(t)$ is negative because the gate is inverting. When the magnitude of the sensitivity is greater than one, the gate is noise-unstable.

model containing only four parameters.

For our purposes, we limit our analytic modelling to standard cells with cell inputs which only connect to transistor gates. Moreover, our modelling will be valid only if the channel-connected components (CCCs)[1] reached from the inputs (those determining the noise stability of the inputs) do not contain pass transistors. While this requirement is generally satisfied by the overwhelming majority of logic gates in standard-cell libraries, we will consider in Section 4 how this model might be extended to the more complex case in which cell inputs and outputs connect directly to FET channels. For the purposes of our cell-level static noise analysis tool, we choose to descend to the transistor level when these conditions are not met by the cell.

The proposed model characterizes not only the noise stability of the standard-cell input but allows evaluation of the entire sensitivity function $S(t)$. In particular, we can find the peak value of $S(t)$ even for circuits which are not driven beyond unity-gain magnitude. Our characterization techniques focus on accurately predicting peak sensitivity up to a magnitude between 0.5 and 1. The model is also accurate across a broad range of possible input noise waveforms and is broadly applicable to both static and dynamic circuit styles. In Section 2, we introduce the model and demonstrate how it is applied in the context of a commercial static noise analysis engine. Section 3 provides detailed analysis of model regression on one of the library elements of a typical standard-cell library. We conclude and offer possible extension to handle channel-connected inputs and outputs as future work in Section 4.

2 Noise stability modelling

The cell models described in this paper are applied in the context of a standard-cell-centered version of a commercial static noise analysis tool, similar to that described in Reference [5]. In the standard-cell context, the tool is principally

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[1]A CCC is a group of transistors connected together by their sources or drains.

focussed on calculating the coupling noise on the interconnect between cells and verifying that this noise does not violate the noise stability of any of the receiving gates. Power-supply differences between driving and receiving gates can be considered with an overall dc offset to the noise. More general static noise analysis techiques consider the propagation of noise from logic-gate input to output. By enforcing conservative noise sensitivity targets, this propagated noise can be kept negligibly small in practice and is, therefore, ignored as part of the cell-level implementation of static noise analysis.
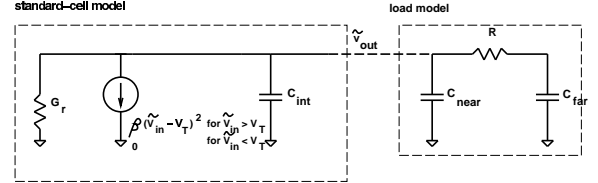

Figure 2: Four-parameter circuit model for noise stability characterization.

Noise can be classified by its magnitude relative to the power and ground rails[5]. There are four choices corresponding to the two voltage references and two senses (positive and negative) relative to these references:

- V_H noise decreases a node voltage below the supply level;

- V_H^* noise increases a node voltage above the supply level;

- V_L noise increases a node voltage above the ground level; and

- V_L^* noise decreases a node voltage below the ground level.

Instead of modifying the model to account for these different types, we choose to define noise by a canonical effective waveform, $\tilde{v}_{in}(t)$, and a type label. The actual voltage on the node $v_{in}(t)$ can then be determined as follows. For V_L noise, $v_{in}(t) = \tilde{v}_{in}(t)$, while for V_L^* noise, $v_{in}(t) = -\tilde{v}_{in}(t)$. For V_H noise, $v_{in}(t) = V_{DD} - \tilde{v}_{in}(t)$, while for V_H^* noise, $v_{in}(t) = \tilde{v}_{in}(t) - V_{DD}$.

For each canonical noise waveform $\tilde{v}_{in}(t)$ of a given type appearing at a given input, the cell model must calculate $S(t)$. To enable characterization, a specific time-domain abstraction is required for the $\tilde{v}_{in}(t)$. We choose a simple two-pole model (with poles p_1 and p_2) and a dc-offset V_{dc}:

$$\tilde{v}_{in}(t) = V_{dc} + ke^{-p_1 t} - ke^{-p_2 t} \qquad (1)$$

Before invoking the cell model to determine $S(t)$ or $\tilde{v}_{out}(t)$, the input waveform (as determined primarily from the coupling noise calculation) must be "collapsed" to this form. We do this with an AWE-like Padé approximant. First, the dc offset is extracted from $\tilde{v}_{in}(t)$ (that is, we determine the value of V_{dc});[2] the resulting waveform then has initial and steady-state values of zero. The waveform is then translated so that the first significant nonzero value occurs at $t = 0$. We then calculate the first three time moments, m_0, m_1, and m_2 and match them to the moments of $ke^{-p_1 t} - ke^{-p_2 t}$ in the Laplace domain.

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[2]In practice, the bookkeeping is such that is already separate since this accounts for supply variation between driver and receiver.

Cell characterization for noise stability

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Abstract

Verifying whether a digital standard-cell design is functional in the presence of interconnect coupling noise is an important concern to ASIC designers. Determining whether the coupling noise occuring on a node is excessive requires comparing this noise against the dynamic noise margins of the receiving gates. The noise stability requirement, introduced in the context of transistor-level static noise analysis, is a technique for quantifying these ac noise margins. In this paper, we describe a technique for modelling noise stability in the form of a four-parameter rule which can be used to characterize the cells of a digital standard-cell library.

1 Introduction

Because of increasing interconnect densities, faster clock rates, more aggressive use of high-performance circuit families, and scaling threshold voltages, noise has become a metric in the design of digital integrated circuits of comparable importance to area, timing, and power[1]. When noise acts against a normally static signal, it can transiently destroy the logical information carried by the node in the circuit. If this ultimately results in incorrect machine state stored in a latch, functional failure will result.

Calculating noise on a node without an understanding of how much noise a given node can tolerate is of little value, but the problem of deciding how much noise a node can tolerate before functional failure is possible is a difficult one. The traditional criterion is to examine the dc noise margins of the receiving circuits, requiring that the peak noise appearing on the node be less than this dc noise margin[2, 3, 4]. Circuit designers are well aware of the fact that dc noise margins, however, are much too conservative to apply against the magnitude of pulse noise sources (such as those produced by interconnect coupling), because they fail to consider the fact that logic gates also act as low-pass filters.

In fact, the *dynamic* noise margins are very dependent on the exact time-domain characteristics of the noise and the tuning of the gate to its load capacitance. Circuits are less sensitive to noise that is sharply pulsed than to noise that is more dc-like. Circuits are also less sensitive to pulsed noise when they are "slow," that is, more poorly tuned for delay against their loads. To account for dynamic noise margins, circuit designers sometimes introduce an "ac noise margin" which is a multiple (usually 2-3) of the dc noise margin. This approach is dangerous since the choice of multiple is very dependent on technology and the types of circuits being considered.

The concept of noise stability was introduced as a means of precisely quantifying dynamic noise margins within the context of transistor-level static noise analysis[5]. This noise stability condition is as follows: *Every restoring logic gate, when acted upon by a noise stimulus, must have a time-domain dc-noise sensitivity that is always less than one.* We illustrate this sensitivity calculation for an inverter in Figure 1. The noise $v_{in}(t)$ "biases" the inverter, producing an output waveform $v_{out}(t)$. The time-domain dc-noise sensitivity $S(t)$ is given by:

$$S(t) = \left. \frac{\partial v_{out}(t)}{\partial V_{dc}} \right|_{V_{dc}=0}$$

This sensitivity examines the subsequent amplification of additional fluctuations of the lowest possible frequency content (i. e. purely dc). If the magnitude of $S(t)$ ever exceeds one, then the gate is noise-unstable, and the associated $v_{in}(t)$ violates the dynamic noise margins of the gate. We note that $S(t)$ is negative because the gate is inverting. V_{dc} is a fictitious source added for the purposes of the sensitivity calculation. Any "real" dc noise will be included in $v_{in}(t)$. In the limit that $v_{in}(t)$ is entirely dc noise, the noise stability requirement defines worst-case static dc noise margins by the usual -1-slope points of the voltage transfer characteristic. If v_{out} approaches the opposing rail, a "two-humped" sensitivity curve is possible as the gate switches completely through the high-gain region and back again.

Even in cases in which a noise-stability violation is not noted, the peak value of $S(t)$ is a useful metric for determining the amount of noise margin left in the design. Circuits with low noise sensitivities (typically of magnitude much less than 0.1) have margin to trade-off noise immunity for area, power, or speed. As sensitivities approach unity magnitude (typically of magnitude greater than 0.5), these sensitivities will increase rapidly in the presence of any finite amount of additional input noise as the logic gate enters the high-gain region of its transfer characteristic. As a result, circuits with sensitivities greater than 0.5 in magnitude (even though they may not be violations) probably require more margin to account for process uncertainties.

In traditional standard-cell ASIC design flows, the transistor-level circuits may not always be available for noise stability analysis. Moreover, on large flat designs, there may not be the capacity to perform detailed transistor-level analysis. Because of these considerations, we have found it useful (and necessary) to have an analytic, rule-based method for characterizing the noise stability of standard cells. We have already considered the other aspects of a standard-cell-type rule in the hierarchical approach to static noise analysis described in Reference [6]. In particular, the output strength of a cell can be characterized by pull-up and pull-down resistances, necessary to calculate coupled noise on the output. In this earlier work, the noise sensitivities of the inputs pins of heirarchical blocks were represented by static dc noise margins. In this paper, we show how the complete noise stability of a cell input can be characterized with a simple