On-Chip Circuit for Measuring Period Jitter and Skew of Clock Distribution Networks

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Abstract –**A circuit for on-chip measurement of period jitter and skew of clock distribution is described. The circuit uses a single latch and a voltage-controlled delay element. The circuit is evaluated in a stand-alone pad frame, where a jitter resolution of about 1 ps is demonstrated, and is incorporated in a 2 GHz clock distribution network to obtain on-chip period jitter and clock skew measurement.**

Index terms
Jitter, period jitter, on-chip measurement, built-in self test, clock distribution, clock skew.

I. INTRODUCTION

With clock and data rates in the multi-GHz range, there is an increasing demand for measuring and controlling jitter. With cycle times substantially less than 1 ns, jitter must be kept in the low ps range. While conventional instruments such as oscilloscopes and time interval analyzers can measure jitter with the required accuracy, such measurements require that high bandwidth off-chip drivers (OCDs) be dedicated for such purposes, and measurement equipment must be connected to chips through high frequency probes or packages. This severely limits both the number of measurements points on a circuit and the number of samples tested.

As a result, there is great interest in developing small, accurate on-chip jitter measurement circuits [1-5]. Two types of jitter are generally considered, as illustrated in Fig. 1. The first, shown in Fig 1a, is tracking (or long-term) jitter, in which a clock signal's jitter is compared to a reference signal. This type of jitter is relevant to the case of several sub-circuits or chips being synchronized to a single clock. The second type, shown in Fig. 1b, is period jitter, in which the variation of the period of the signal is compared on successive cycles. This type of jitter is important, for example, in establishing latch hold time requirements, and for determining timing requirements for I/O data circuits where there is no accompanying clock. Period jitter is generally smaller than long-term jitter, making measurement more demanding. In addition to jitter measurement, complex chips also face the problem of clock skew, that is, different ends of the clock distribution may have different average time differences, due to process, temperature or voltage variation.

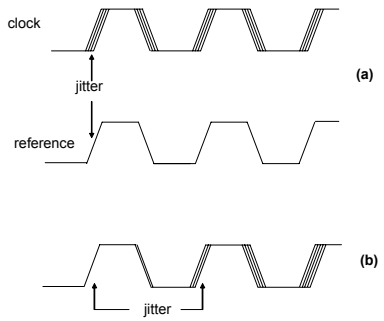

Fig. 1. Illustration defining tracking jitter (a) and period jitter (b).

This paper reports a small on-chip circuit which measures both period jitter and skew. Its performance is demonstrated in a stand-alone design, and it is incorporated in a novel clock distribution circuit where it provides the measurements necessary to evaluate the design. This is the first time such an on-chip jitter measurement circuit has been used for real measurement in an integrated circuit.

II. MEASUREMENT CIRCUIT

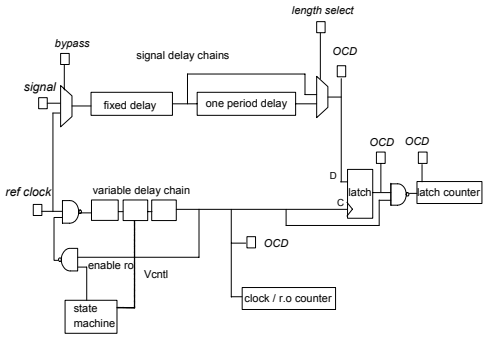

Fig. 2. Block diagram of the stand-alone jitter measurement circuit.

The jitter measurement circuit is based on the single latch design previously demonstrated in [5]. A block diagram is shown in Fig. 2. The concept of the circuit is that the signal to be measured becomes the data input to an edge-triggered latch, while the reference signal becomes the clock input. Both signals first pass through delay chains. The delay of the clock signal is varied by voltage control, such that its arrival time at the latch extends from before the data signal to after the data signal. As such, the number of counts from the latch indicates what fraction of the data signal distribution arrives before the clock. By counting this fraction as a function of the clock delay, a cumulative distribution (CDF) of the data arrival time is generated. The probability distribution function (PDF) of the data is recovered by differentiating the CDF. Setting the variable delay path as a ring oscillator enables a delay-to-voltage calibration, so on-chip data with the correct time scale are obtained with no additional adjustments required. An extra path in the data delay chain switches in a fixed delay (equal to one period), so the latch measures the jitter between a first signal and one delayed by a period, that is, period jitter.

The circuit was implemented in two designs. One was a stand-alone pad cage design for evaluation and characterization. In this design, signals were applied though high bandwidth probes to test the response of the measurement circuit to known jitter, and also to measure the impact of power supply noise. Second, the circuit was also incorporated at several test points in a clock distribution circuit, where it was used to measure jitter and skew. Some differences in the designs of these implementations are listed in Table 1.

Table 1.

design	*technology*	*function*	*clock period*	*delay elements*
stand-alone	0.09 μm	tracking or period jitter	900 ps	inverters
embedded	0.18 μm	period jitter and skew	500 ps	differential buffers

III. MEASUREMENT EXAMPLES

A. Characterization in stand-alone circuit

The circuit in the stand-alone pad frame was designed for a fixed delay of about 900 ps, for a target frequency of about 1.1 GHz. It was implemented in 0.09 μm technology operated at 1.1 V. It is noted that jitter of the falling edge, which indicates the impact of jitter on duty cycle, can be measured at half target frequency, hence some of the illustrative data here are obtained for this condition.

The circuit was evaluated by applying a signal of known jitter through the high frequency probes to the circuit, and operating the circuit as described. To create input jitter, a pulse generator with external phase delay control was used. The input jitter was measured conventionally, with a real-time oscilloscope for comparison.

Fig. 3. Oscilloscope measurement of period jitter for clock frequency of 540 MHz. The oscilloscope measured jitter of 1.7 ps.

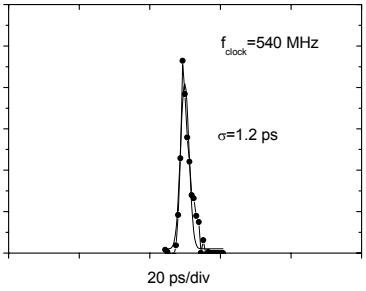

Fig. 4. On-chip measurement of period jitter for clock frequency of 540 MHz to compare with Fig. 3. A Gaussian fit is used to estimate standard deviaton.

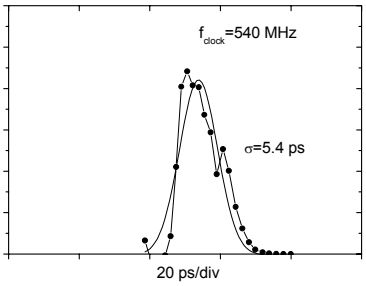

Fig. 5. On-chip measurement of period jitter with jitter added by delay modulating pulse generator. f_{clock}=540 MHz. A Gaussian fit is used to estimate standard deviation.

The response of the circuit to a signal with no added jitter is shown in Figures 3 and 4. The oscilloscope shows rms jitter of 1.7, while the on-chip circuit shows about 1.2 ps. This is the intrinsic jitter resolution limit in this implementation. The on-chip measurement shows better resolution, because, unlike the oscilloscope, there is no contribution due to trigger jitter.

With Gaussian noise of bandwidth 10 MHz applied to the pulse generator, the jitter spectrum is broadened, as shown in Fig. 5. The on-chip circuit matches the oscilloscope histogram (not shown) quite well, with rms jitter of 5.5ps vs 5.7 with the oscilloscope.

Fig. 6. Oscilloscope measurement of period jitter with jitter added by delay modulating pulse generator. f_{clock}=540 MHz.

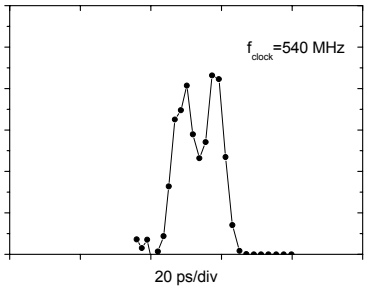

Fig. 7. On-chip measurement of period jitter with jitter added by delay modulating pulse generator. f_{clock}=540 MHz, to compare to Fig. 6.

A more complex jitter distribution was created by modulating the phase delay of the pulse generator with a sinusoidal signal, resulting in the histograms of Fig, 7 and 8. The agreement is excellent.

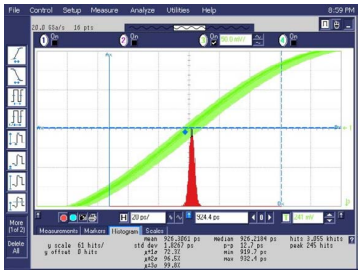

Fig. 8. Oscilloscope measurement of period jitter for clock frequency of 1080 MHz. The oscilloscope measured jitter of 1.8ps.

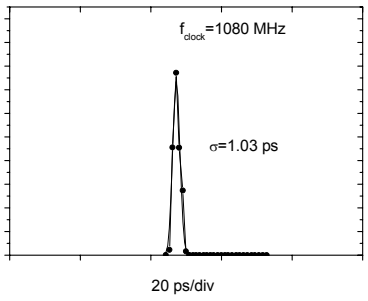

Fig. 9. On-chip measurement of period jitter for clock frequency of 1080 MHz. A Gaussian fit is used to estimate standard deviation.

The intrinsic resolution of the on-chip circuit at 1080 MHz is determined by comparing Fig. 8, with a corresponding on-chip measurement in Fig. 9. No reduction in resolution results from higher frequency operation. Again the on-chip circuit is slightly better than the oscilloscope measurement. In fact, it was shown by observing various test points of the circuit that power supply noise of the off-chip drivers actually created some jitter, so that an implementation without the drivers could be expected to have even smaller resolution than demonstrated here.

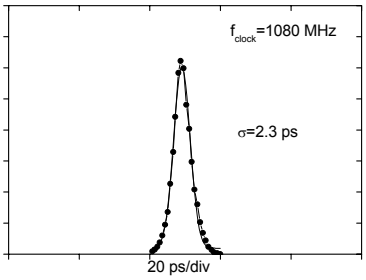

Fig. 10. On-chip measurement of period jitter with Gaussian noise applied to delay chain power supply. f_{clock}=1080 MHz. A Gaussian fit is used to estimate standard deviation.

Because of the extra path delay used to compare cycle-delayed edges, the circuit is susceptible to jitter artifacts created by power supply noise. In the of the construction of the test circuit, such noise could be applied directly in order to observe the impact. An example of this effect is shown in Fig, 10, where Gaussian noise of 30 to 100 mV is applied to the delay chain power supply. This results in a broadening of the spectrum to 2.3 ps. While this is a concern, it is noted that in the stand-alone circuit, simple inverters were used for the delay chains, making them particularly sensitive to power supply voltage. A practical use of this measurement technique, as shown below, uses delay elements with high power supply rejection ratio (PSRR).

A differential (sense-amplifier) flip- flop [6] is used in both implementations of this circuit because it has a very small metastability window and setup time. The simulated metastability window of the latch is less than 0.1 ps. This result could be limited by the accuracy of the simulation, but it does suggest the latch has excellent metastability, consistent with the high resolution demonstrated by measurement.

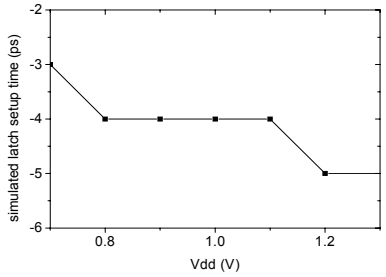

Fig. 11. Simulated setup time of the latch as a function of Vdd.

The latch is also shown to be quite insensitive to supply voltage. Simulations of a 1.0 V latch, shown in Fig. 11, show that the setup time of the latch stays relatively constant over a wide range of power supply variation, thus introducing little or no jitter in a noisy environment.

B. Use of circuit to measure clock tree jitter and skew

In order to measure period jitter of a novel clock distribution circuit targeted for 2GHz**,** the measurement circuits were designed along with the clock circuit. This circuit was designed in 0.18 μm, 1.8V technology. The clock circuit was designed for very low period jitter, hence the need for high-resolution on chip measurement. In order to avoid sensitivity to power supply noise, the delay elements in this implementation were differential buffers, with the variable elements controlled by their tail currents and pFET gate voltage [7].

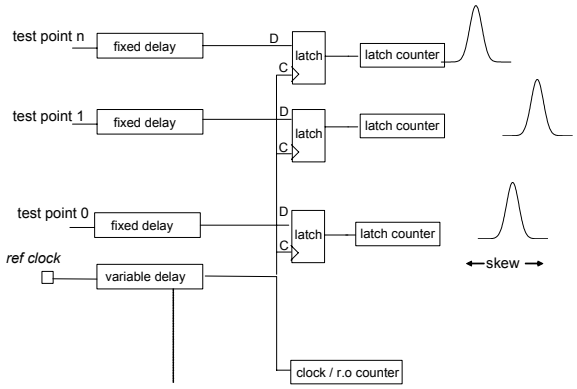

Fig. 12. Simplified block diagram of implementation of jitter measurement circuit for measuring clock-to-clock skew.

To measure clock skew, modified measurement circuits were placed at two points on the clock tree, however, they shared a common variable delay chain so that the timing difference, or skew, between test points is given by the difference of the means of the generated histograms. The concept of skew measurement is shown in the block diagram of Fig. 12**.**

An example of measured point-to-point clock skew is shown in Fig. 13. In this figure, the cumulative jitter distribution measured by the on-chip circuit is measured at two points on the clock tree. Instead of differentiating the data to recover the original distribution, it is sufficient to measure just the shift of the midpoint of the CDF. In this case, this shift is about 16 ps. Clearly the on-chip circuit has more than enough accuracy to measure skew of this magnitude. The accuracy is, of course. related to the jitter resolution, which is on the order of 1 ps.

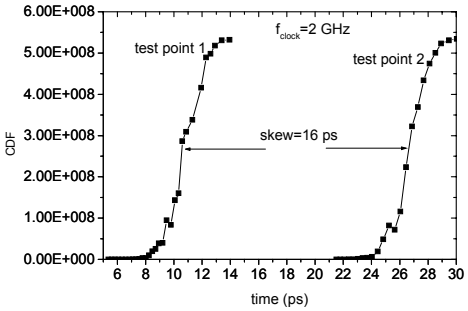

Fig. 13. Example of measured point-to-point skew using the on-chip measurement circuit.

SUMMARY

A new on-chip period jitter measurement circuit has been presented. By using two delay lines differing by one clock period, and a single latch, the circuit measures the cumulative probability distribution due to jitter. By differentiating, the original distribution is recovered. In addition, use of a common time base for multiple placements of the circuit enables measurement of clock skew. The circuit has been demonstrated in a stand-alone test site for characterization, and has been used to measure the jitter and skew of an experimental clock network. It has a demonstrated resolution of about 1ps up to 2 GHz clock frequency.

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