Design of Coupled Power Inductors with Crossed Anisotropy Magnetic Core for Integrated Power Conversion

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***Abstract*—Design and partial microfabrication of a coupled power inductor is presented for use in high power-density integrated voltage regulators (IVR). The proposed inductor uses many laminations of uniaxial, high-permeability magnetic material where the orientation of anisotropy between successive laminations is rotated to provide an effectively isotropic core. The high permeability core allows for an inductance density of 200nH/mm^2, while coupling between phases prevents magnetic saturation and allows a current density as high as 11A/mm^2 according to quasi-static finite-element-analysis (FEA) simulations. The coupling factor, inductance and resistance of the device are optimized for operation in a four-phase integrated buck converter switching at 100MHz.**

I. Introduction

Energy consumption is now the primary constraint on performance in modern microprocessors. Across the full spectrum of computing platforms from mobile devices to high-end servers, computational performance is limited by tolerable power dissipation. A promising method to increase performance-per-watt of digital integrated circuits (ICs) is dynamic voltage and frequency scaling (DVFS), where the supply voltage and clock frequency are adjusted transiently to match required workloads, resulting in substantial power savings [1,2]. The benefit of DVFS is multiplied with a granular implementation that supports many supply voltages, enabling optimization of operating voltages on a per core (or more granular) basis. Unfortunately, the board-level voltage regulator modules (VRMs) currently employed do not scale well to meet high current demands at low voltages across many different voltage domains.

Integrated voltage regulators (IVRs) are a promising alternative to VRMs, as they offer the ability to provide many dynamically scalable power supplies in a cost-effective manner [3-12]. IVRs offer the added benefit of reducing the PCB footprint of an IC by eliminating the need for board-level regulators, as well as alleviating constraints on the power distribution network (PDN) by delivering power at lower current levels, subsequently reducing the impact of the PCB and package PDN impedance. Switched-capacitor IVRs have been investigated as a means to provide these benefits, showing high efficiency at reasonable current densities but have done so only at fixed conversion ratio and without addressing transient requirements [3-5]. Meanwhile, switched-inductor (buck) converters have shown high current densities and efficiencies with a continuous range of conversion ratios [6-12]. The principal roadblock for implementation of switched-inductor IVRs is integration of the power inductors. In this paper, we will present the design of a magnetic-core coupled power inductor that efficiently provides high current density and efficiency and should, therefore, enable implementation of switched-inductor IVRs on a large scale.

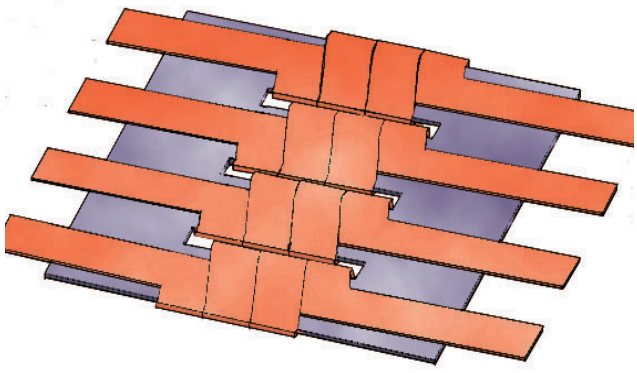

Figure 1. Proposed four phase coupled power inductor, copper windings (red), CZT core (grey)

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II. Review of Integrated Power Inductor Development

A. *Figures of Merit*

In buck converters, the inductor serves as an energy reservoir, where electrical energy is periodically stored in a magnetic field and subsequently released to the load at a lower electrical potential. As a result, the significant figures of merit for a candidate power inductor are the inductor quality factor and inductance density [13].

Unfortunately, using inductance density and quality factor as the only figures of merit obscures important limitations and capabilities of candidate inductor technologies. Specifically, inductance density ignores the issue of magnetic saturation that can occur in magnetic core inductors carrying large DC currents. For example, an inductor topology may achieve a high inductance density by incorporating a large number of turns, however the saturation current, I_{SAT}, for such a device would likely be low, substantially reducing its viability for use in a power converter. Maximum energy density, E_{DNS}, may be suggested as an alternative benchmark to inductance density, where L is self inductance and A is the total area of a single inductor

$$E_{DNS} = \frac{LI_{SAT}^2}{2 \times area}. \tag{1}$$

Unfortunately, E_{DNS} as a figure of merit is not suitable for comparing coupled inductor topologies where power is not only stored in the device but is also transformed through the magnetic coupling. As a result, the maximum energy delivered to the load during a switching period, T_{SW}, can be larger than the maximum energy storage of the inductor.

Likewise, quality factor is an inadequate indicator of the potential efficiency that can be achieved with a candidate power inductor because it overlooks the broadband nature of the inductor current during operation in a switching regulator. The spectral content of an inductor's current will have strong components not only at the switching frequency, f_{SW}, but also at DC and potentially at harmonics of f_{SW} for the case of coupled inductors.

For the purposes of comparing candidate inductor topologies for IVRs, we propose the complimentary figures of merit, maximum current density, I_{DNS}, and effective inductor efficiency, $\eta_{L,EFF}$. I_{DNS} can be determined as the maximum average inductor current, $I_{L,MAX}$, divided by the area of the inductor. The maximum average inductor current, $I_{L,MAX}$ is a function of the inductor saturation current and the worst-case inductor current ripple, $\Delta I_{L,P\text{-}P}$:

$$I_{L,MAX} = I_{SAT} - \frac{1}{2}\Delta I_{L,P-P} \tag{2}$$

For the case of air-core inductors, I_{SAT} should be the peak inductor current as limited by electromigration or heat. Thus the maximum current density is

$$I_{DNS} = \frac{I_{L,MAX}}{area}. \tag{3}$$

Determination of $\Delta I_{L,P\text{-}P}$ will vary with inductor topology; for the case of uncoupled inductors, $\Delta I_{L,P\text{-}P}$ is given by

$$\Delta I_{L,P-P} = \frac{V_{IN} T_{SW} D(1-D)}{L} \tag{4}$$

where V_{IN} is the converter input voltage and D is the converter duty cycle [14] and should be chosen as 0.5 for a worst-case current ripple.

Inverse coupling between adjacent inductors can be used to increase the maximum current, assuming that all inductors are carrying the same DC current. $I_{L,MAX}$ is then modified to include coupling as

$$I_{L,MAX} = \frac{I_{SAT}}{1+(N_C-1)k} - \frac{1}{2}\Delta I_{L,P-P} \tag{5}$$

where N_C represents the number of coupled inductors in a coupled set. When N_C=2, the relationship between inductor terminal voltages and currents is

$$\begin{bmatrix} A & B \\ B & A \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \frac{\partial}{\partial t} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}$$

$$A = \frac{1}{L(1-k^2)} \quad B = \frac{-k}{L(1-k^2)} \tag{6}$$

where L is the self-inductance of a single phase, k is the coupling coefficient between two coupled inductors commonly chosen around −0.8 for N_C=2 and v_1, i_1, v_2 and i_2 are, respectively, the voltages across and currents through the two inductors of the coupled pair. The worst-case inductor current ripple for such a configuration occurs when D=0.25 or 0.75 and can be found as

$$\Delta I_{L,P-P} = \frac{V_{IN} T_{SW}}{4L(1-k^2)}\left(0.75 + 0.25k\right) \tag{7}$$

We repeat this analysis for the case of four symmetric coupled inductors, N_C=4, where each inductor is coupled to the other three with the same coupling coefficient. The inductor voltage-current relationships can be approximated as

$$\begin{bmatrix} A & B & B & B \\ B & A & B & B \\ B & B & A & B \\ B & B & B & A \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = \frac{\partial}{\partial t} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix}$$

$$A = \frac{1+2k}{L(1+2k-3k^2)} \qquad B = \frac{-k}{L(1+2k-3k^2)}. \tag{8}$$

Note that in the case of N_C symmetric inversely coupled inductors, the strongest coupling coefficient achievable is $-1/(N_C-1)$. The worst-case inductor current ripple for N_C=4 occurs when D=0.375 or 0.625 and can be found as

$$\Delta I_{L,P-P} = \frac{V_{IN} T_{SW}}{8L(1+2k-3k^2)}\left(1.875 + 5.125k\right) \tag{9}$$

Similar analysis can be conducted to determine the worst-case inductor current ripple for any N_C.

The effective inductor efficiency $\eta_{L,EFF}$ should be determined as a ratio between power delivered to the load and the power input to the inductors. The major loss contributors in inductors are DC and high-frequency resistive losses, which account for winding resistance, core eddy currents, and magnetic hysteresis. Thus, $\eta_{L,EFF}$ is generalized to

$$\eta_{L,EFF} = \frac{I_{L,MAX} V_{OUT}}{I_{L,MAX} V_{OUT} + R_{DC} I_{L,MAX}^2 + R_{fsw} \dfrac{\Delta I_{L,P-P}^2}{12}} \tag{10}$$

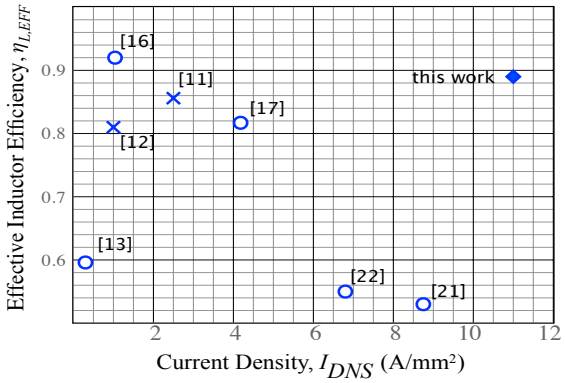

Figure2. Graph of maximum current density and effective inductor efficiency for notable works on integrated power inductors. × measured, ○ computed from measured quantity, ♦ simulated. Note: some device parameters were estimated when not available in print.

where R_{DC} is the DC inductor resistance, R_{fsw} is the inductor resistance at f_{SW} and V_{OUT} is the IVR output voltage. In (10), the rms power of the current waveform is approximated as that of a triangle wave with peak-to-peak current ripple of $\Delta I_{L,P-P}$.

Within these two figures of merit, V_{IN}, T_{SW} and V_{OUT} remain as free variables that are independent of the power inductors yet have an influence over their performance according to I_{DNS} and $\eta_{L,EFF}$. Typical value for these parameters are V_{IN}=2V, T_{SW} =100MHz and V_{OUT}=1V, based on recent work on switched-inductor IVRs[6-12].

B. *Previous Work*

Spiral inductors, or other topologies that can be integrated into the back-end-of-line (BEOL) of a typical CMOS process, are typically too resistive to provide efficient on-chip power conversion at reasonable current densities [15]. The efficient use of SMT air-core inductors [16], which can provide a current density of ~1.0A/mm^2, has been successfully demonstrated in [6-10]. However, an IVR incorporating discrete SMT inductors is poorly suited for power conversion with core-level granularity, because the size and discrete nature of the SMT devices limits scalability.

Integrated thin-film magnetic core power inductors will be highly scalable and dense, relieving the complications associated with integrated buck converters. Initial attempts to produce such devices demonstrate a higher inductance density than air-core inductors, but magnetic saturation significantly limited the currents they can support [13,17]. The introduction of coupling between magnetic core inductors mitigates the issue of magnetic saturation [18,19] while enabling improved transient response [20]. A 16-phase buck converter using coupled stripe inductors with sputtered $Ni_{80}Fe_{20}$ cladding has been demonstrated delivering 25A with a current density of ~8A/mm^2 and a peak efficiency of 76% [11,21]. An alternate implementation using coupled race-track inductors with electroplated $Ni_{45}Fe_{55}$ [22] integrated into an eight-phase IVR by chip stacking achieves a maximum current density of ~1.7A/mm^2 and a peak efficiency of 74% with current density of 1A/mm^2 where approximately 74% of losses occur in the inductor [12]. The performance of these power inductors, according to the metrics defined in Section IIb, is given in Fig. 2.

III. Design of Thin-Film Magnetic Coupled Power Inductors

The power inductor topology proposed in this paper is shown in Fig. 1. The device resembles that from [18,19] with a geometry similar to a ladder, where each of the rungs is a solenoid inductor that is coupled through the stringers of the ladder. In the proposed device, many laminations of anisotropic $Co_{91.5}Zr_{4.0}Ta_{4.5}$ (CZT) compose the core where the orientation of anisotropy is rotated between successive pairs of laminations to produce an effectively isotropic core. An example of the magnetic laminations is shown in a SEM image in Fig. 3 where an insulating bi-layer of SiO_2 and Ta separates magnetic laminations; the SiO_2 layer suppresses eddy currents while the Ta helps to smooth roughness in the sputtered SiO_2 layer. Coupling between inductors is employed to avoid magnetic saturation and improve converter transient response [18-20]. This inductor topology differs from previous work in that the core is planar and the magnetic lamination thickness and spacing is optimized to avoid the formation of domain walls as well as eddy currents, which can increase losses at high frequency.

A. *Optimization of Inductor Magnetic Core*

In general, the proposed inductor structure is advantageous because the planar nature of the core allows for reduced losses. While laminating the core with insulating layers will suppress losses due to eddy currents, the coercivity, or hysteresis, of the magnetic material is still a source of loss in the inductor. Coercivity is a result of two magnetic processes: single-domain rotation and domain wall motion. We can reduce the coercivity associated with single-domain rotation by material selection and optimization of deposition conditions. We can reduce losses from domain wall motion by optimizing the spacer layer between adjacent laminations of magnetic material that have the same orientation of anisotropy in order to promote flux closure, or dipolar-coupling, between the adjacent layers, which suppresses domain formation [23].

We have chosen $Co_{91.5}Zr_{4.0}Ta_{4.5}$ (CZT) as the material system as it has been demonstrated to offer high saturation magnetization, low coercivity and relatively high resistivity [13]. CZT also has a larger induced anisotropy field (Hk) than most compositional variants of Ni-Fe, which is needed to overcome shape anisotropy in this particular core geometry.

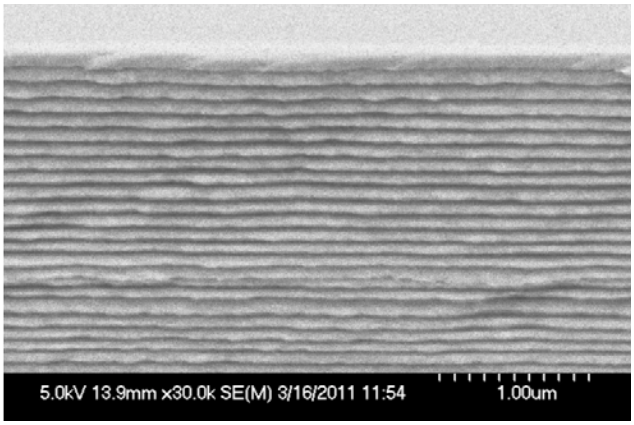

Figure 3. SEM image of magnetic laminations

Dipolar-coupling between adjacent layers reduces (or even eliminates) the presence of domain walls within the core and consequently minimizes any losses associated with domain wall motion. Fig. 4 shows magnetic force microscopy (MFM) images of single-layer and dipolar-coupled bi-layer magnetic material patterned as a tile; domain walls are clearly present in the single layer while absent in the bi-layer. To avoid formation of domain walls, the spacing between magnetic laminations should be ~10nm so that the path of magnetic flux, which is induced by the easy axis magnetization, may be easily closed between adjacent layers while avoiding the formation of pin-holes in the insulating spacer layer that would allow the laminations to be exchange-coupled. Likewise, the 10nm spacer layer should be thick enough to outweigh any convexity that may occur in the films and would result in orange-peel coupling between layers. The likely consequence of either exchange or orange-peel

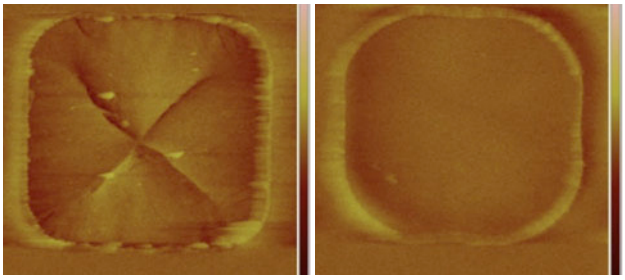

Figure 4. MFM images of a single magnetic layer (left) and a dipolar coupled bi-layer (right), note domain walls do not form in bi-layer

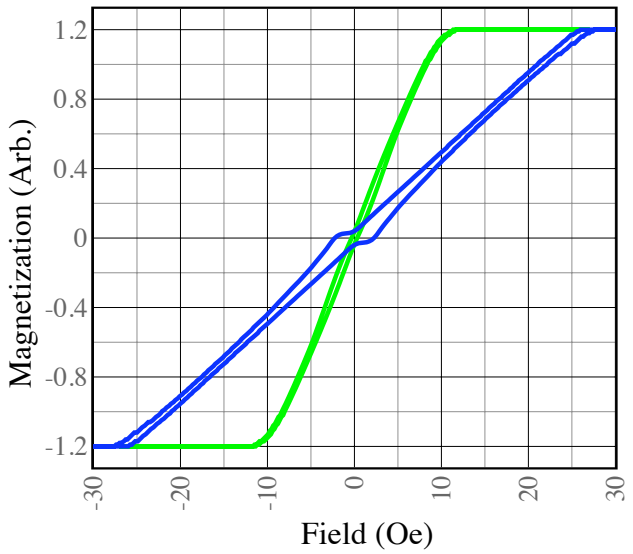

Figure 5. Magnetization curves for easy (blue) and hard (green) axis for patterned CZT bi-layers

coupling between adjacent magnetic layers is the formation of domain walls within the core. The easy-axis and hard-axis magnetization curves of a CZT bi-layer, patterned as a 400μm-by-100μm bar are shown in Fig. 5. The abnormal shape of the easy axis curve around 0Oe is the result of the bi-layer's resistance to nucleation of additional domains within each layer when the two layers are dipolar-coupled. With a core structure that assumes a non-planar topography it would be difficult to avoid orange-peel coupling, and hence core losses due to hysteresis may be a dominating loss mechanism for the power converter.

B. *Fabrication Description and Constraints*

The inductor fabrication is composed of four major deposition steps; the sequential deposition of the bottom copper windings, magnetic core, copper vias and top copper windings, with several depositions of thin films for insulating, adhesion or seeding interspersed.

The copper interconnect is chosen for its low resistivity and is patterned with a damascene process. In the damascene process, copper is electroplated onto a copper seed layer that was deposited on a permanent insulating polymer layer and has been patterned with trenches. The copper is plated to a thickness where it overfills the trenches. The substrate then undergoes chemical mechanical polishing that planarizes the surface by removing copper down to the top of the insulating layer, leaving a planar surface where copper has filled the trenches in the insulator. It is important that the substrate surface be planar to within a few nano-meters following deposition of the first metal layer in order to avoid orange-peel coupling in the magnetic layers. In order to reduce the resistive losses in the inductor, it is desirable to achieve a large cross sectional area for the copper windings, however, limitations in the lithography process constrain the maximum copper thickness to around 5μm, with resolution limiting the minimum space that can be reliably patterned in a copper film to ~5μm.

The laminated nature of the core material precludes the use of most conventional processing techniques for patterning thin films. A chemistry that is able to selectively attack CZT, Ta and SiO_2 is not available to our knowledge, and so the lithography techniques for patterning the magnetic core are constrained to ion milling and lift-off. In the proposed inductor topology, magnetic flux travels in the same plane as the core, and in order to reduce the reluctance for this it is desirable to achieve a large cross sectional area for the magnetic core. Unfortunately, ion milling is impractical for patterning relatively thick (several μm) metal films, because it is not selective and would therefore require a mask of similar thickness as the core itself.

Therefore, we employ a bi-layer photoresist lift-off process, where a thick layer of the polymer LOR 30B is spun onto the substrate and soft-baked, followed by a thin layer of Microposit S1811 photoresist that is also spun on and soft baked. The photosensitive polymer bi-layer is then patterned by optical contact lithography with the desired core geometry. When the photoresist mask is developed, the underlying LOR 30B will dissolve faster than the S1811 photoresist, forming an undercut in the resist mask, which will allow lift-off lithography to be conducted with films that are ~0.8× the thickness of the LOR 30B layer. LOR 30B is highly viscous and at low spin speeds can achieve thicknesses of ~5μm, thus with the combined LOR + S1811 photoresist reaching a maximum thickness of around 6μm the core thickness is limited to ~4.0μm.

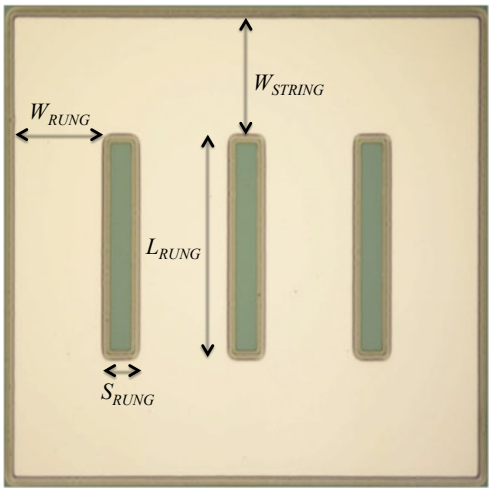

Figure 6. Fabricated CZT core with optimized dimensions.

C. *Inductor Design Optimization*

A reluctance-based analytical model has been derived for an inductor structure similar to the proposed device in [19]. This model is effective at predicting the general behavior of the inductor currents and their coupled interactions, but unfortunately, it does not produce usable solutions for key device parameters, such as inductance and coupling coefficient, in terms of physical dimensions of the device.

Despite these limitations, the model can, in principle, facilitate numerical design optimization as demonstrated in [19]. Unfortunately, for the case of thin film inductors, we find discrepancies in these analytical models when compared with finite element analysis (FEA) simulations. This is a result of poor analytical modeling of the reluctance for flux paths outside of the plane of the magnetic core, which are substantial in thin film inductors and can result in reduced coupling coefficient.

With our inability to analytically optimize the inductor design, we have relied on iterative simulations in the FEA simulator Maxwell for design optimization. Fig. 6 shows a fabricated CZT core with significant design dimensions indicated. The rung width, W_{RUNG}, rung space, S_{RUNG}, rung length, L_{RUNG}, and stringer width, W_{STRING}, for the final design are 120µm, 50µm, 270µm and 140µm respectively so that the total device dimensions are 630µm by 550µm occupying 0.35mm^2. Increasing W_{RUNG} will reduce the reluctance for magnetic flux in the core at the expense of winding length, which would increase DC resistance. S_{RUNG} is desired to be as small as possible in order to maximize coupling between adjacent inductors. However, this space must be large enough to accommodate the winding vias which will be placed between the rungs. Reducing L_{RUNG} reduces the magnetic path length and increases inductance at the expense of winding cross section, which increases DC resistance. Increasing W_{STRING} helps to improve coupling between inductors, but with diminishing effect, while it consumes more total area and hence reduces current density.

IV. Simulated Results

Simulations in Maxwell indicate a peak current density for the device of 11A/mm^2 limited by magnetic saturation. The inductor resistance as a function of frequency is shown in Fig. 7, where the DC resistance is 93mΩ. A consequence of the thin laminations and relatively high resistivity of CZT is that very little eddy current losses occur at frequencies of interest and thus both inductance and coupling coefficient remain flat as frequency increases. The average L_{self} across the four phases at 100MHz is 18.4nH, with a coupling factor of −0.2 between each of the phases. The simulator includes eddy current losses in both the core and the windings along with estimated hysteretic losses but does not consider more complicated effects such as domain motion. Simulated time-domain waveforms of the inductor current ripple are shown in Fig. 8 where D=0.625. Coupling between the inductor phases reduces inductor current ripple and also keeps the peak flux density below the saturation magnetization (M_s) of CZT, 1.3T, as verified by field solutions from the transient simulation. The simulated current density and effective inductor efficiency are shown in Fig. 2 for comparison against previous works.

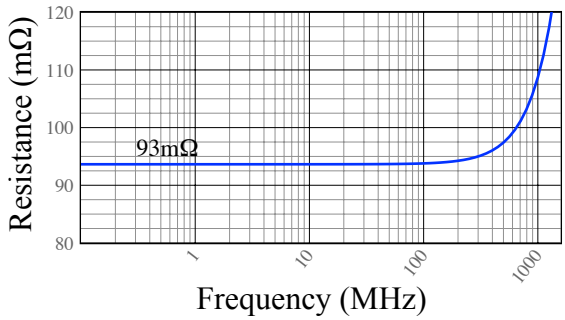

Figure 7. Frequency domain simulation of inductor resistance in the proposed four phase inductor

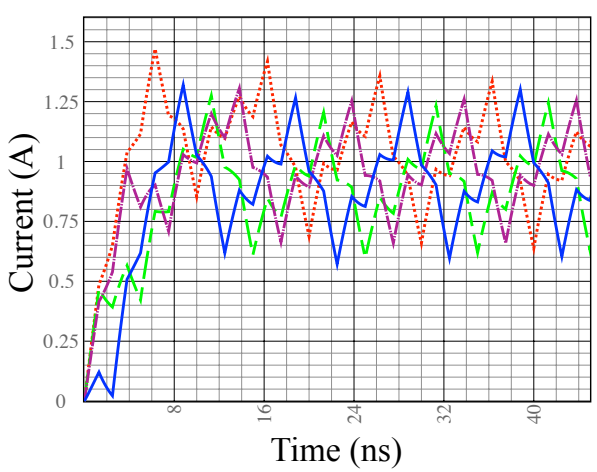

Figure 8. Time domain simulation of the inductor current in the proposed four phase coupled inductor

V. CONCLUSIONS

The proposed inductor uses high-quality laminations of CZT that are dipolar coupled to prevent the formation of domain walls and consequently improve effective inductor efficiency. The device fabrication steps have been optimized to provide thick copper layers for the inductor windings and thick magnetic cores to increase inductance density while maintaining the quality of the magnetic layers. Fabrication of complete devices is ongoing. FEA simulations have been used to optimize current density and effective inductor efficiency. Simulated results indicate that the proposed inductor is a promising candidate for future IVRs.

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REFERENCES

[1] J. Howard, *et al.*, "A 48-Core IA-32 Processor in 45 nm CMOS Using On-Die Message-Passing and DVFS for Performance and Power Scaling," *Solid-State Circuits, IEEE Journal of,* vol. 46, pp. 173 - 183, 2011.

[2] W. Kim, *et al.*, "System level analysis of fast, per-core DVFS using on-chip switching regulators," High Performance Computer Architecture, 2008. HPCA 2008. IEEE 14th International Symposium on (2008) pp. 123 – 134

[3] G. Patounakis, *et al.,* "A fully integrated on-chip DC-DC conversion and power management system," *Solid-State Circuits, IEEE Journal of*, vol.39, no.3, pp. 443- 451, March 2004

[4] H. Le, *et al.*, "A 32nm fully integrated reconfigurable switched-capacitor DC-DC converter delivering 0.55W/mm2 at 81% efficiency," *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International,* pp. 210 - 211, 2010.

[5] L. Chang, *et al.,* "A fully-integrated switched-capacitor 2:1 voltage converter with regulation capability and 90% efficiency at 2.3A/mm2," *VLSI Circuits (VLSIC), 2010 IEEE Symposium on,* pp. 55 - 56, 2010.

[6] G. Schrom, *et al.*, "A 480-MHz, multi-phase interleaved buck DC-DC converter with hysteretic control," *Power Electronics Specialists Conference*, 2004, Vol.6, pp. 4702-4707

[7] P. Hazucha, *et al.*, "A 233-MHz 80%-87% efficient four-phase DC-DC converter utilizing air-core inductors on Package," *IEEE Journal of Solid-State Circuits,* Jan 1 2005.

[8] G. Schrom, *et al.,* "A 100MHz Eight-Phase Buck Converter Delivering 12A in 25mm2 Using Air-Core Inductors," *Applied Power Electronics Conference, APEC 2007 - Twenty Second Annual IEEE,* pp. 727 - 730, 2007.

[9] G. Schrom, *et al.,* "A 60MHz 50W Fine-Grain Package Integrated VR Powering a CPU from 3.3V," *Applied Power Electronics Conference - Special Presenation,* Feb 25 2010.

[10] N. Sturcken, *et al.*, "An integrated four-phase buck converter delivering 1A/mm^2 with 700ps controller delay and network-on-chip load in 45-nm SOI," *Custom Integrated Circuits Conference (CICC), 2011 IEEE* , vol., no., pp.1-4, 19-21 Sept. 2011

[11] J. T. DiBene, *et al.*, "A 400 Amp fully Integrated Silicon Voltage Regulator with in-die magnetically coupled embedded inductors," *Applied Power Electronics Conference - Special Presenation,* Feb 25 2010.

[12] N. Sturcken, *et al.,* "A 2.5D Integrated Voltage Regulator using Coupled Magnetic Core Inductors on Silicon Interposer Delivering 10.8A/mm^2" *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International*, (to appear)

[13] D. Gardner, *et al.,*"Review of On-Chip Inductor Structures With Magnetic Films," Magnetics, IEEE Transactions on (2009) vol. 45 (10) pp. 4760 – 4766

[14] R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*, 2nd ed. Norwell, MA: Kluwer, 2001.

[15] J. Wibben and R. Harjani, "A High-Efficiency DC–DC Converter Using 2 nH Integrated Inductors," Solid-State Circuits, IEEE Journal of (2008) vol. 43 (4) pp. 844 – 854

[16] "Chip Inductors" *0302PA Series Datasheet,* Coilcraft Inc.

[17] Lee, *et al*., "Fabrication and Analysis of High-Performance Integrated Solenoid Inductor With Magnetic Core. Magnetics," IEEE Transactions on (2008) vol. 44 (11) pp. 4089 – 4095

[18] Wong, *et al.* "Performance improvements of interleaving VRMs with coupling inductors," IEEE Transactions on Power Electronics (2001) vol. 16 (4) pp. 499-507

[19] Li, *et al., "*Coupled-inductor design optimization for fast-response low-voltage DC-DC converters," Applied Power Electronics Conference and Exposition, 2002. APEC 2002. Seventeenth Annual IEEE (2002) vol. 2

[20] Li, *et al*., "Using coupled inductors to enhance transient performance of multi-phase buck converters," Applied Power Electronics Conference and Exposition, 2004. APEC'04. Nineteenth Annual IEEE vol. 2 pp. 1289–1293

[21] P.R. Morrow, *et al.,*"Design and Fabrication of On-Chip Coupled Inductors Integrated With Magnetic Material for Voltage Regulators," *Magnetics, IEEE Transactions on* , vol.47, no.6, pp.1678-1686, June 2011

[22] N. Wang, *et al.*, "Integrated On-chip Inductors With Electroplated Magnetic Yokes," paper EH-01 at the 56th Magnetism and Magnetic Materials (MMM) Conference (2011).

[23] J. Slonczewski, *et al.,* "Micromagnetics of Laminated Permalloy Films," IEEE Transactions on Magnetics (1988) pp. 1-10