Characterization and modeling of graphene field-effect devices

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Abstract

The novel electronic properties of graphene, including a linear energy dispersion relation and purely two-dimensional structure, have led to intense research into possible applications of this material in nanoscale devices. In this paper, we review the unique electronic properties of graphene that give it the potential for high-frequency electronic applications. We then present the latest results on the current-voltage characteristics of top-gated graphene FETs. These devices show unique characteristics related to the ambipolar nature of the graphene channel. In addition, the devices show very high saturation velocities, suggesting the possibility for superior high frequency performance. Our initial devices have transconductances as high as 150 μS/μm despite low on-off current ratios, making the devices very suitable for analog/RF applications.

1. Introduction

Field-effect transistors based on carbon nanotubes have been the subject of intensive research for the last decade[1-5]. The limited control over the chirality and diameter of nanotubes (and the associated electronic bandgap) remains a major problem. A further limitation is the requirement for tightly packed arrays of nanotubes to achieve current levels comparable to silicon field-effect devices[6]. Graphene offers many of the advantages of carbon nanotubes—carrier mobilities of up to 2 x 10^4 cm^2/V-sec in substrate supported devices[7-9] and large (~10^8 A/cm^2) critical current densities[10]—without the need for assembling large parallel arrays of nanotubes to achieve high on currents.

At the same time, however, graphene has unique electronic properties that make it different from semiconductors, presenting both challenges and opportunities.

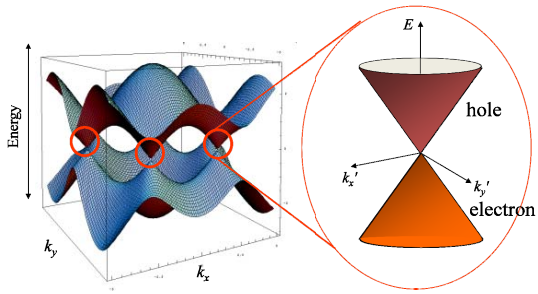

Figure 1. Band structure of graphene.

2. Electronic structure of graphene

Graphene, a two-dimensional (2D) honeycomb structure of carbon, has a unique bandstructure that results in unusual transport properties[11]. In particular, graphene is a zero-bandgap semiconductor as shown in Fig. 1 with an energy dispersion relation (π electrons in the first Brillouin zone) given by:

$$E(\boldsymbol{k}) = s\hbar v_F|\boldsymbol{k}|$$

where *s=+1* in the conduction band and *s=-1* in the valence band and $v_F \sim 10^8 cm/s$ is the Fermi velocity. The $|\boldsymbol{k}| = 0$ point is known as the Dirac point and if often referenced to *E=0*. The bands are twofold spin degenerate (g_s=*2*) and also carry a twofold valley degeneracy (g_v=*2*). The charge carriers in the two-dimensional channel can change from electrons (Fermi energy, $E_F > 0$) to holes ($E_F < 0$) with the application of an electrostatic gate. Impurities adsorbed to the graphene surface can also dope the structure.

The zero-bandgap of graphene limits achievable on-off current ratios ($\boldsymbol{I_{on}/I_{off}}$). Bandgaps of up to 400 meV have been introduced by patterning graphene into narrow ribbons[12-14] although this has resulted in significant mobility degradation and fabrication challenges. Bandgaps can also be achieved through the application of perpendicular electric fields to bilayer graphene structures[15, 16], but these gaps are far less than 400 meV and would lead to significant band-to-band tunneling.

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In a 2D graphene field-effect structure, the modulation of the Fermi level in the channel is determined not only by the electrostatic capacitance (C_e) of the gate dielectric but by the quantum capacitance (C_q) of graphene, which considers density-of-state effects in determining modulation of charge. The two capacitors act in series, leading to an effective top gate capacitance of $C_{top} = \frac{C_q C_e}{C_q + C_e}$. C_q is sheet-carrier-concentration-dependent and is given by $C_q = \sqrt{\frac{n}{\pi}} \frac{e^2}{v_F \hbar}$. [17] Since the devices are fabricated on a conducting substrate, this can act as a backgate. The quantum capacitance does not have a significant effect on the effective back-gate capacitance because the back-gate capacitance per unit area is substantially smaller than for the top gate.

3. Field-effect device fabrication

One of the principle challenges in graphene technology is materials synthesis. The most promising growth techniques are based on high-temperature silicon desorption from SiC surfaces[18]. As a result, most devices are fabricated from graphene mechanically exfoliated from Kish graphite, a labor-intensive process that produces very small flakes of graphene. [10] These are usually exfoliated on a 300-nm thermally grown SiO_2 wafer, which allows optical recognition of the graphene sheets. Raman spectroscopy is generally employed to verify that these are single graphene sheets.

In our case, top-gated graphene field-effect transistors (GFETs) begins with the identification of strips of graphene with widths between 1-5 µm. Cr/Au electrodes are patterned lithographically to define source and drain contacts. A low-temperature atomic-layer-deposition (ALD) process is used to directly grow 15-nm HfO_2 onto the graphene sheet as a high-κ gate dielectic for the local top gate. Because graphene does not have any dangling bonds on its surface, chemical-vapor-deposition- (CVD-) based growth techniques are often difficult. Some have suggested functionalizing the graphene first with NO_2 as part of the growth procedure.[19] In our case, growth is most likely due to physiosorption, which is enhanced by the low-temperature growth procedure we employ.

4. Field-effect device characteristics

We have measured top-gated GFETs based on this high-κ HfO_2 gate dielectric.[20] Despite $I_{on}/I_{off} \sim 7$, high transconductances and current saturation are achieved, making this device well-suited for analog applications. The GFETs (Fig.2a) have source and drain regions that are electrostatically doped by the back gate, which enables control over the contact resistance and threshold voltage of the top-gated channel. Fig.2b shows a GFET structure with 3-µm source-drain separation, a 1-µm top gate length, and a device width of 5 µm. We review representative measurement and modeling results for a similar device with a width of 2.1 µm.

The back-gate capacitance (C_{back}) is approximately 12 nF/cm^2 (thickness of 285 nm, κ ~ 3.9). Sheet carrier concentrations (electrons or holes) in the source and drain regions can be approximated by $n \cong \sqrt{n_0^2 + \left(C_{back}\left(V_{gs-back} - V_{gs-back}^0\right)/e\right)^2}$, where $V_{gs-back}^0$ is the back-gate-to-source voltage at the Dirac point in these regions and n_0 is the minimum sheet carrier concentration as determined by disorder and thermal excitation[21, 22]. $V_{gs-back}^0 \cong 2.7\,V$, indicating slight p-type doping, most likely due to impurities adsorbed to the graphene. Under the top gate, carrier concentrations are determined by both the front and back gates, $n \cong \sqrt{n_0^2 + \left(\left[C_{back}\left(V_{gs-back} - V_{gs-back}^0\right) + C_{top}\left(V_{gs-top} - V_{gs-top}^0\right)\right]/e\right)^2}$ with $V_{gs-top}^0 \cong 1.45\,V$, where $C_{top} \cong 552\,nF/cm^2$ is the effective top-gate capacitance per unit area. If one takes the top-gate capacitance as being the series combination of the electrostatic capacitance (C_e) of the gate dielectric and the quantum capacitance (C_q) and for $C_q \cong 2\,\mu F/cm^2$, $C_e \cong 762\,nF/cm^2$, which is slightly less than the 944 nF/cm^2 predicted for the HfO_2 gate insulator (thickness of 15 nm, κ ~ 16), probably due to surface impurities trapped between the HfO_2 and graphene, increasing the effective gate insulator thickness.

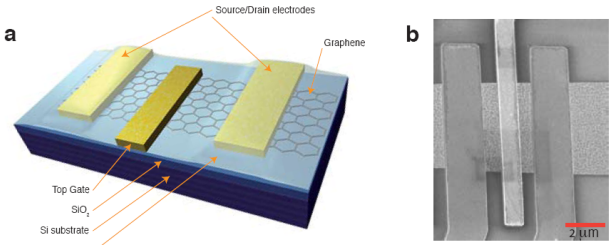

Figure 2. Basic top-gated graphene FET design. (a) schematic depiction of a graphene FET on a Si/SiO_2 substrate with a heavily doped Si wafer acting as a back-gate and a gold top-gate. (b) SEM micrograph showing a representative graphene top-gated FET. The Cr/Au top-gate of this device is 1 µm long, with 3 µm spacing between the source-drain contacts.

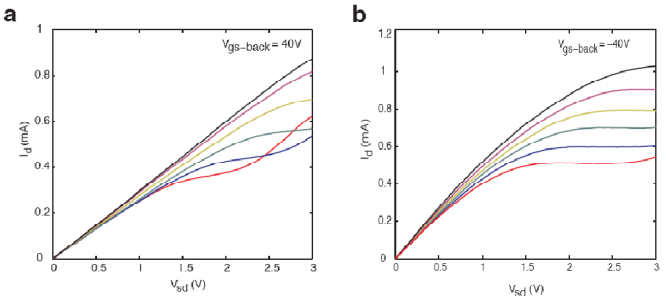

Figure 3. Current-voltage characteristics of GFET device: (a) drain current (I_d) as a function of source-to-drain voltage (V_{sd}) for V_{gs-top}=-0.3V,-0.8V,-1.3V,-1.8V,-2.3V, and -2.8V (from bottom to top) for $V_{gs-back}$=40 V; (b) I_d as a function of V_{sd} for V_{gs-top}=-0.3 V,-0.8V, -1.3V, -1.8V, -2.3V, and -2.8V (from bottom to top) for $V_{gs-back}$=-40 V.

Figs. 3a and 3b show the measured I_d as a function of V_{sd} (for different V_{gs-top} voltages) at $V_{gs-back}$ of 40V and -40V. To understand these curves, we focus first on the I_d curve from Fig. 3a for V_{gs-top}= *-0.3V*, which shows a pronounced "kink" in the characteristic, shown in more detail in Fig. 4a. Similar to the features observed in ambipolar semiconducting nanotubes FET[23],these kinks in the I_d characteristics signify the presence of an ambipolar channel. The carrier concentration in the channel, shown schematically in Fig. 4b for different points in the I-V trace, is calculated using a field-effect model: $n(x) = \sqrt{n_0^2 + \left(C_{top}(V_{gs-top} - V(x) - V_0)/e\right)^2}$, where $V_0 \cong V^0_{gs-top} + (C_{back}/C_{top})(V^0_{gs-back} - V_{gs-back})$ functions as a device threshold voltage, controlled by the back-gate; x is the distance along the graphene channel; and $V(x)$ is the potential in the channel. For the device in Fig 3, with channel length L, $V(L) = V_{sd}$, so that for $V_{sd} \leq V_{sd-kink} \cong V_{gs-top} - V_0$ current is carried by holes throughout the length of the channel (Fig 3b-I). The linear relationship between V_{gs-top} and $V_{sd-kink}$ is also evident in the contour plots of Fig. 2c and 2d. For $V_{sd} = V_{sd-kink}$, the vanishing carrier density produces a "pinch-off" region at the drain (Fig 3b-II) that renders the current in the channel relatively insensitive to V_{sd} and results in the pronounced kink seen in the I-V characteristic. ForV_{sd}>$V_{sd-kink}$, the minimal density point resides in the channel, producing a "pinch-off" region that moves from source to drain with increasing drain bias magnitude(Fig. 3b-III). In this bias range the carriers in the channel on the source side of the minimal density point are holes, while those on the drain side are electrons. The voltage drop across the "hole" portion of the channel remains fixed at $V_{sd-kink}$ while the voltage drop across the "electron" portion increases as V_{sd}-$V_{sd-kink}$. In this ambipolar regime, the pinch-off point becomes a place of recombination for holes flowing from the source and electrons flowing from the drain. Because there is no bandgap, no energy is released in this recombination.

For the I-V curves at $V_{gs-back}$= *-40V* and V_{gs-top} < *-0.8 V* (Fig. 2b), the device shows flat saturating I-V characteristics (high-field regime for a unipolar channel). To accurately model these characteristics, the drift velocity must be assumed to saturate at some value v_{sat} for electric fields beyond a critical electric field (E_{crit}). This is consistent with the carrier drift velocity eventually saturating due to optical-phonon scattering, as in the case of metallic nanotubes[24] [25]. For values of V_{gs-top} sufficiently negative, such that $V_{sd-kink}$> $E_{crit}L$, the I-V characteristics show a strongly saturating behavior in the unipolar region with the kink indicating a transition to an ambipolar channel. Large enough electric fields are reached in the channel at the drain end for the holes to reach saturation velocity, resulting in an I_d that becomes independent of V_{sd}.

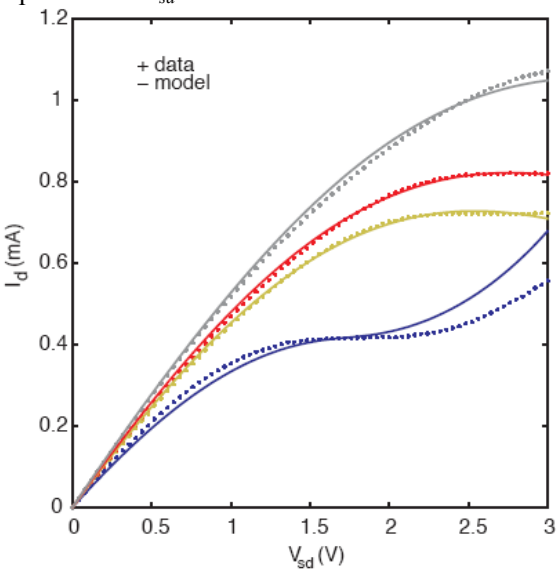

Figure 4. Model (solid) and measured (dashed) I_d-V_{sd} curves are compared for $V_{gs-back}$=-40 V at V_{gs-top}=0V, -1.5V, -1.9V, and -3V (from the bottom to the top)

With this consideration, the current in the channel is expressed by[26]:

$$I_d = \frac{W}{L}\int_0^L en(x)v_{drift}(x)dx \qquad (1)$$

Where L is the channel length and W is the channel width. Current continuity forces a self-consistent solution for the potential $V(x)$ along the channel. We approximate the carrier drift velocity (v_{drift}) by a velocity saturation model[27]:

$$v_{drift} = \frac{\mu E}{1+\frac{\mu E}{v_{sat}}} \qquad (2)$$

where v_{sat} is the saturation velocity of the carriers. For simplicity, we assume that both electrons and holes are characterized by the same μ and v_{sat} values in our model. A closed-form analytical expression for I_d can be derived from these expressions. Fig. 4 shows a comparison of this model with the measured data at

$V_{gs\text{-}back}$= *-40 V*; the model has been implemented in Verilog-A as described in Section 5. As input parameters, the fit uses a low-field mobility of 550 cm^2/V-sec, a minimum sheet carrier density of 0.5 x 10^{12} cm^{-2}, and source-drain series resistances of 700 Ω. v_{sat} for holes is found to vary between 6.3 x 10^6 cm/sec at high densities (at $n \cong 10 \times 10^{12} cm^{-2}$) and 5.5 x 10^7 cm/sec at low densities (near n=n_0). We find that v_{sat} shows a linearly increasing trend with $n^{-1/2}$ given by the simple relation $v_{sat} = v_F \left(\frac{\hbar\Omega}{E_F}\right)$ with $\hbar\Omega$ designating the relevant optical phonon energy.[20] We find $\hbar\Omega$ to be close to the 55 meV surface phonon energy of SiO_2[28, 29] and consistent with the observation of the effect of this phonon energy on temperature-dependent low-field mobility.[30] This phonon energy is significantly below the 200 meV longitudinal zone boundary phonon of intrinsic graphene,[31] suggesting that the saturation velocity in future generations of graphene transistors may be augmented by choosing different substrates with higher phonon energies.

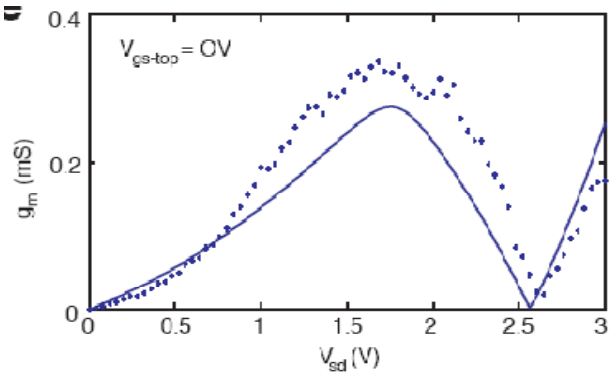

Figure 5. Small-signal transconductance (g_m) as a function of drain-to-source voltage (V_{sd}) for $V_{gs\text{-}top}$=-2.9V.

Figs. 5 show the small-signal device transconductance $(g_m \triangleq (\partial I_d/\partial V_{gs-top})|_{V_{sd},V_{gs-back}})$ as a function of V_{sd} for $V_{gs\text{-}top}$ = 0 V. Model and measurement show good agreement. g_m values exceed 320 µS/µm (~150 µS/µm) for these 2.1-µm-channel-length devices at $V_{gs\text{-}top}$*=0 V*, $V_{gs\text{-}back}$*= -40 V*, V_{sd}*=1.6V*. Removing the effect of series resistance, the device's intrinsic transconductance is approximately 833 µS/µm at a v_{sat} value of 5.5 x 10^7 cm/sec. In comparison, velocity-saturated n-channel 65-nm Si MOSFETs deliver transconductances of approximately 1.5 µS/µm with gate capacitances of approximately1.77 µF/cm^2. At this gate capacitance, which is close to graphene's quantum capacitance, the graphene transistor would have a transconductance of more than 2.9 mS/µm. As expected, and as is evident in Fig. 4e, the transconductance goes to zero at V_{sd} =$V_{sd\text{-}kink}$. The highest transconductances are observed in the unipolar regime away from $V_{sd\text{-}kink}$, which can be achieved by proper choice of V_0. Therefore, the device is most likely to be operated in the high-transconductance, velocity-saturated region with V_{sd} below $V_{sd\text{-}kink}$.

The performance potential of graphene comes from its comparatively high v_{sat} value. Silicon, even with the most optimistic assumption on strain and perfectly ballistic channels, will have a v_{sat} limited to 2 x 10^7 cm/sec. [32] The competitive landscape with III-V materials is shown in Table 1. InAs-based HEMTs in particular, offer the possibility for high saturation velocity (because of the low effective mass in InAs) but have relatively poor electrostatics, making scaling to short channel lengths difficult. [33] They are also characterized by relatively large "spacer" layers leading to high series resistances.

Table 1. Comparison of graphene for III-V materials.

	InAs	GaAs	InP	Graphene
Electron effective mass (m^*/m_0)	0.023	0.067	0.077	0
Electron mobility (300K, N_D=10^{17}cm-3)	16000	4600	2800	20000
Electron saturation velocity (x 10^7 cm/sec)	4.0	2.2	2.2	> 5
Energy bandgap (eV)	0.36	1.42	1.35	0

5. CAD challenges

The most obvious challenges for computer-aided design are in the compact modeling of these devices, since they present very different current-voltage behavior than semiconductor-based FETs. In Fig. 6, we show a simple large-signal device model that we have implemented in Verilog-A to describe the behavior of our GFET devices. The $I_d(V_{gs\text{-}top},V_{ds})$ relationship is determined by solution of Eqns. 1 and 2. The capacitance model at this early stage includes only the total gate capacitance as the gate-to-source capacitance. More details will be presented elsewhere.[34]

This model predicts f_Ts in excess of 40 GHz for the 0.5µm GFET device of Figs. 3 and 4. RF measurements will also be reported elsewhere.[34]

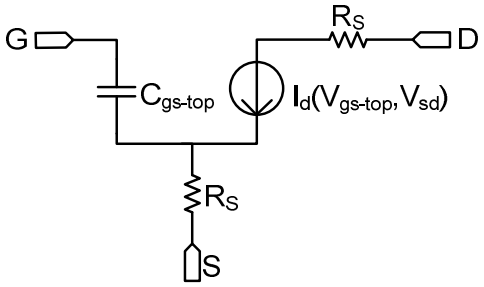

Figure 6. Compact model of graphene FET. $I_d(V_{gs\text{-}top},V_{sd})$ is given by the solutions of Eqns. 1 and 2.

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