Hybrid carbon nanotube-silicon complementary metal oxide semiconductor circuits

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A hybrid technology is presented that combines carbon nanotube field-effect transistors (CNFET) with conventional, silicon-based complementary metal oxide semiconductor (CMOS) technology. The fabrication involves the chemical vapor deposition growth and optical characterization of carbon nanotubes, which are then transferred with lithographic precision onto a commercially fabricated CMOS substrate. In this manner, CNFET devices are fabricated on top of the interconnection network of the CMOS chip, providing a three-dimensional integration of active devices, "sandwiching" wiring, and passives. As a demonstration of this approach, a simple hybrid CNFET/CMOS inverter is fabricated and tested.
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I. INTRODUCTION

Silicon complementary metal-oxide-semiconductor (CMOS) technology is facing increasing challenges in continuing performance gains with channel length scaling due to the growing importance of fringe capacitance parasitics, short-channel effects due to degraded electrostatics, and gate leakage. Silicon technology is focusing on double-gate or finFET technology to improve device parastics and boost device transconductance, high-k gate dielectrics to reduce gate leakage, and uniaxially strained silicon channels to boost ballistic velocities.[1] At the same time, there has been growing interest in carbon nanotubes (CNs) as an alternate channel material for field-effect devices.[2] The advantages here include ballistic velocities that are potentially 50% higher[3] than what can be achieved in strained silicon and inherent "wrap-around" gating of nanotubes which improves short-channel effects and boosts transconductance per unit device width if nanotubes can be packed into dense arrays.

Many challenges remain in the fabrication of carbon nanotube field-effect transistors (CNFET) including relatively primitive fabricated device structures that result in poor subthreshold slopes and high parasitics, Schottky-barrier sources and drains which result in ambipolar FET behavior, and poor control over the properties of the nanotubes used for fabrication. Some progress has been made in these areas including doped contacts[4] and self-aligned device structures.[5] Most of the devices fabricated have been single transistors; very recently an all-CNFET ring oscillator has been demonstrated,[6] although its performance is dominated by parasitics and the resulting voltage waveforms are noisy (due to the low gain of the CNFET devices), requiring spectral analysis.

For any high-frequency operation, devices based on arrays of parallel tubes will be required to achieve large enough transconductance to overcome parasitics. Any cost-effective utilization of CNFET devices will require cointegration with Si CMOS to fully exploit low-cost CMOS transistors wherever possible. There have been previous demonstrations of combined CNFET and Si MOS transistor circuits but these relied on custom fabrication processes.[7,8]

Here, we report on the implementation of a hybrid CNFET/CMOS technology performed as a postprocess on a conventional commercial submicron CMOS run. The fabrication process involves a transfer mechanism that allows carbon nanotubes to be grown and optically characterized (to determine the bandgap, E_g, and chirality) before being transferred with lithographic precision to a conventional CMOS chip, resulting in a three-dimensional integration with CMOS and CNFET devices "sandwiching" the metal interconnection network. This approach represents a general strategy in which high-performance carbon-based devices could

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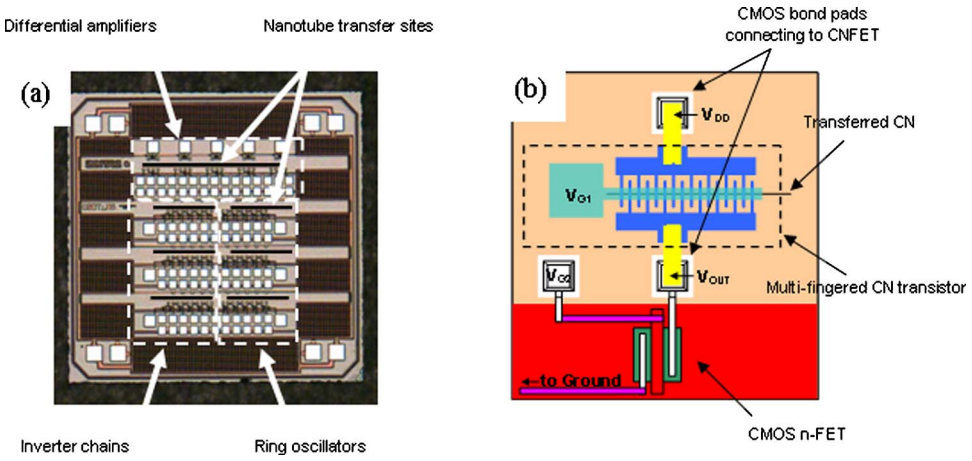

FIG. 1. (a) Die photo of the test CMOS substrate, showing the available sites for tube transfer for hybrid circuit fabrication. (b) Schematic of the CNFET fabricated on the CMOS substrate. The *n* FET is part of the chip commercially fabricated in 0.7 μm technology.

be employed strategically with Si CMOS devices and passives for analog/RF and mixed-signal applications.

II. EXPERIMENT

Figure 1(a) shows a die photo of the commercially fabricated prototype 0.7 μm, three-metal, 5 V CMOS chip used as the "substrate" for CNFET fabrication. Regions are reserved on the die for CN transfer with appropriate pad openings for connections. The die supports the design of several hybrid circuit structures, including ring oscillators and single-stage differential amplifiers in which two CNFET devices fabricated from the same nanotube are used for the differential input pair. We have begun our fabrication and testing with a single hybrid CMOS/CNFET inverter in which the pull down device is a Si *n*-FET and the pull-up device is a CNFET *p*-FET, as shown in Fig. 1(b). While this circuit does not present any circuit advantages, it is the simplest hybrid circuit that can be constructed.

The nanotube transfer process begins with the growth of nanotubes on silicon substrates with slits (width of 70 μm, length of 1 mm) etched completely through the substrate, as shown in Fig. 2(a). Posts on either side of the slit ($\sim$10 μm high and $\sim$20 μm wide) are "stamped" with a Co/Me catalyst. These "seeded" posts promote the growth of individual nanotubes or small bundles and allow for more efficient transfer of the nanotube to a CMOS substrate coated with a conformal top-level Si_3N_4 passivation layer. During CN growth the chip is placed with the slit perpendicular to the gas flow in the chemical vapor deposition reactor such that long tubes are carried downstream over the slit. The freely suspended nanotubes, Fig. 2(a), created by this technique are characterized by Rayleigh and Raman scattering, as described in Ref. 9, to determine the tube diameter, the approximate E_g of semiconducting tubes, and the (n,m) chiral indices (this also indicates whether the tubes are semiconducting or metallic). Figure 2(b) shows the Rayleigh scattering spectra of the two-tube semiconducting bundle used in the inverter.

Following growth and optical characterization, the nanotubes are transferred to the CMOS substrate by aligning the slit over the substrate in a mask aligner and bringing the

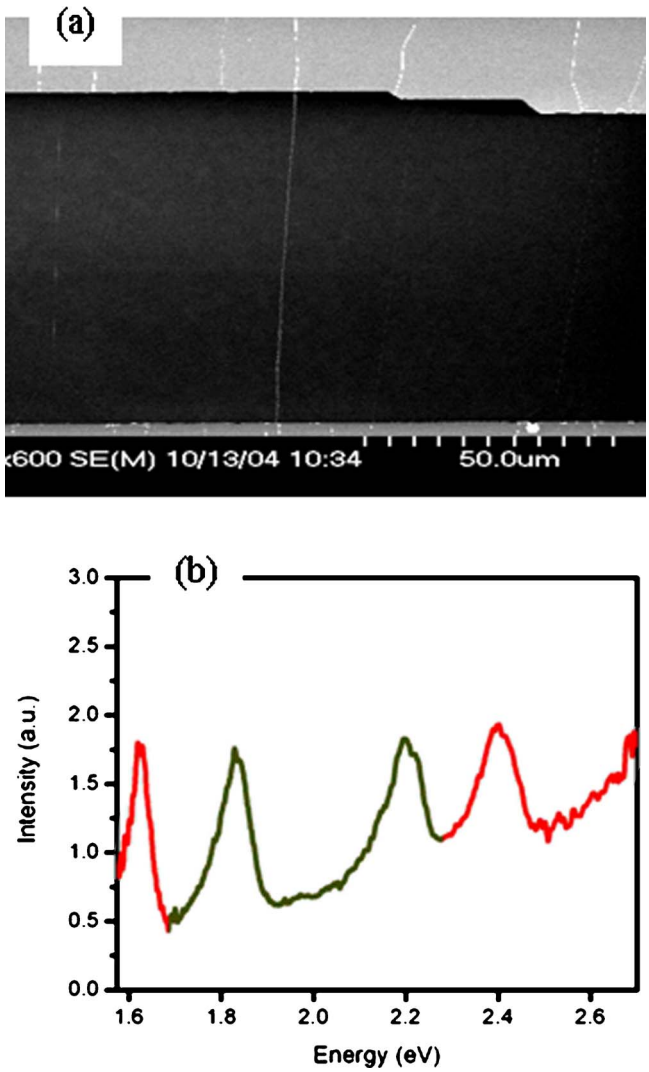

FIG. 2. (a) SEM micrograph of grown two-nanotube bundle traversing the slit substrate. (b) Rayleigh scattering spectra for two-nanotube bundle used for fabrication of the CNFET *p*-FET device. Inner peaks correspond to a (15,14) nanotube. Outer peaks correspond to (24,2) nanotube. Both tubes have 1.99 nm diameter. (Based on analysis of the Rayleigh spectra as described in Ref. 9).

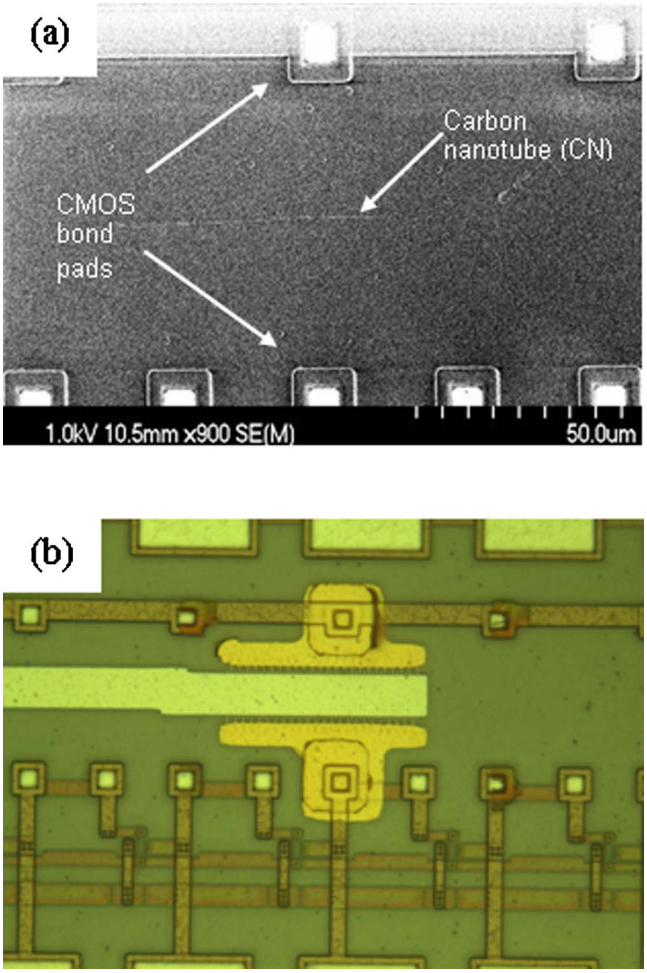

FIG. 3. (a) SEM micrograph of transferred nanotube before device fabrication. (b) Fabricated CNFET *p*-FET device on the CMOS substrate.

tubes into contact with the substrate.[10] The suspended tubes are then covered with a layer of micropipetted photoresist and heated. The growth substrate is then removed, leaving the nanotubes embedded in the photoresist on the target substrate. The photoresist is then dissolved, leaving the nanotube on the CMOS chip. Figure 3(a) shows an scanning electron microscopy (SEM) micrograph of the carbon nanotube transferred onto the CMOS chip prior to any subsequent processing.

After the transfer process, several lithographic steps are used to fabricate the nanotube transistor and connect it to the existing silicon transistors on the substrate. Twenty pairs of source and drain electrodes are patterned along the length of the transferred tube to build a multifingered device. Electron beam lithography is used to pattern source and drain electrodes using polymethyl metacrylate (PMMA) as a resist. Due to the thick dielectric layer of the CMOS chip; a thin layer of aluminum (~15 nm) is thermally evaporated before each electron beam writing step to reduce charging and to enable imaging of the sample surface for alignment purposes. The 500-nm-wide source and drain contacts with a 500 nm channel spacing are patterned, and the PMMA is developed in MIBK:IPA 1:3 for 1 min. (The aluminum layer is removed prior to developing by dipping the sample in a 1*N* solution of NaOH for 10 s.) A 30-nm-thick palladium (Pd) is then deposited by electron beam evaporation, followed by an acetone lift-off. Pd-CNFET Schottky barriers are known to deliver lower contact resistance (compared with other metals) because of higher metal work function, forming a low barrier to the valence band of the nanotube,[11] and enhanced wetting of the nanotube.[12] A second electron beam lithography step is used to "wire" the device to pad openings on the CMOS substrate using Cr/Au (5 nm/80 nm) to form the hybrid inverter. A 30-nm-thick gate dielectric of Al_2O_3 ($\kappa \sim 9.5$) is then grown by atomic layer deposition at 250 °C, followed by electron beam patterning and thermal evaporation of an aluminum gate. Our current process results in large gate-to-drain and gate-to-source overlap capacitances; future experiments will implement a self-aligned CNFET structure to minimize these parasitics and enable us to achieve high-frequency performance. In addition, the gate of the CNFET *p*-FET is not directly wired into the CMOS *n*-FET in the current prototype to allow the introduction of an offset voltage in the gate bias. The fabricated CNFET/Si CMOS circuit is shown in Fig. 3(b).

III. RESULTS

Figure 4(a) shows the measured *I-V* characteristic of the CNFET devices in the hybrid inverter. The I_D-V_{GS} curve (with a V_{SD} of 5 mV) shown in Fig. 4(b) illustrates the semiconducting behavior of the device. These device characteristics are comparable to those reported in Ref. 6, which fol-

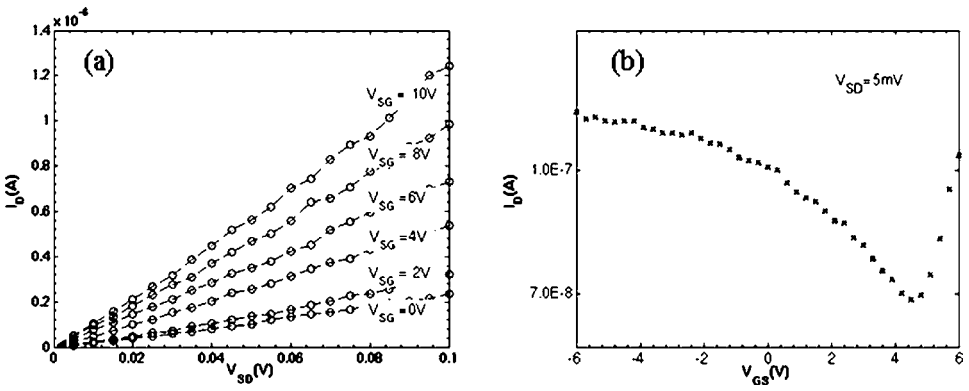

FIG. 4. (a) Measured *I-V* characteristics of the CNFET *p*-FET integrated into the hybrid inverter. No saturation is evident in this plot as it is taken over a restricted range of V_{SD}. (b) The I_D-V_{GS} curve of the same CNFET.

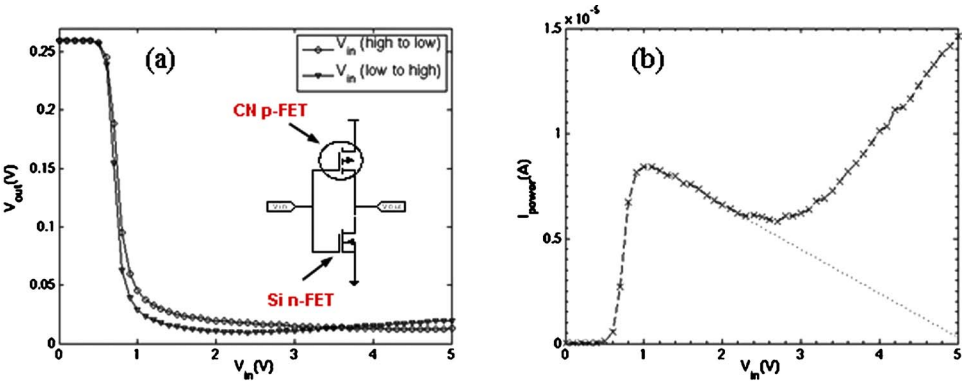

FIG. 5. (a) Voltage transfer characteristic of hybrid CNFET/CMOS inverter operating at V_{DD}=0.26 V. (b) Supply current for the inverter as a function of V_{in}.

lowed similar device fabrication with relatively thick gate dielectrics. The I_D-V_{DS} family of curves in Fig. 4(a) shows a transconductance of 0.129 μS at V_{SD}=0.1 V. The drain current does not yet saturate at these restricted values of V_{SD}. Figure 5(a) shows the measured voltage transfer characteristic (V_{out} as a function of V_{in}) of the circuit operating with a V_{DD} of 0.26 V. The input voltage of the inverter has a 5 V swing for this measurement to achieve an I_{on}/I_{off} ratio greater than 10 for the CNFET device. Because of the lack of threshold voltage control for the CNFET *p*-FET, an offset voltage of −5 V is applied to the gate; this positions the I_D minimum of Fig. 4(b) at zero V_{GS}. Figure 5(b) shows the measured supply current as a function of V_{in}. Although we would expect a very low static current dissipation at high input voltages as shown by the dotted line, we observe an additional increase in the current as shown. This increase in the supply current at higher input voltages is due to the ambipolar properties of the CNFET.

IV. CONCLUSIONS

A hybrid technology is demonstrated that involves the fabrication of carbon nanotube transistors as a postprocess on a conventional Si CMOS fabrication run. A transfer procedure that begins with optically characterized tubes avoids high-temperature processing of the CMOS dice and guarantees the electrical properties of the CNs being employed. The dc characteristics of a simple hybrid CMOS inverter are demonstrated. Future work will incorporate more advanced CNFET structures including self-aligned and doped source and drain regions. We will also fabricate other hybrid circuits including differential pairs, ring oscillators, and SRAM cells.

ACKNOWLEDGMENTS

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