Variability and yield improvement: rules, models, and characterization

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ABSTRACT

Yield and variability are becoming detractors for successful design in sub-90-nm process technologies. We consider the fundamental lithography and process issues that are driving variability and yield and the role of design rules in future processes. We examine the importance of layout-aware modeling and layout regularity, including advantages and cost. Characterization structures for examining the electrical effects of device-level variability are discussed as well as circuit techniques for mitigating variability and yield challenges.

1. YIELD AND VARIABILITY

Yield includes both catastrophic and parametric yield. Design rules are traditionally employed to mitigate the effects of random defects, which are generally modeled with critical areas, breaks, and bridges. Rules are written to widen spaces or widths as a function of run length. For contacts and vias, common layout rules ensure redundancy, avoid isolation, and increase overlaps. "Recommended" rules augment required rules to further improve yield[1]. Process variability, leading to parametric yield loss, is becoming an equally critical concern. These sources of variability include global statistical variation (including process gradients) and local random variability, or "mismatch" (e.g. due to line-edge roughness and random doping fluctuations). Global statistical variations are often categorized as lot-to-lot, wafer-to-wafer, on-wafer (die position in wafer), and within die (across-chip variation). Systematic effects that are often treated as random because they are inadequately modelled include printing effects due to subwavelength lithography, which leave device characteristics sensitive to geometry and local environment, and proximity effects, such as STI stress, well proximity, and contact stress relief.

ICCAD'06, November 5-9, 2006, San Jose, CA

What is ultimately variable is a set of physical parameters (p) which include doping levels and profiles, lateral dimensions such as polysilicon critical dimensions and overlaps, and vertical dimensions such as oxide thicknesses and junction depths. For a given parameter, p_j,

$$p_j = p_{jo} + \delta p_{jc} + \delta p_{ju}(g)$$

where p_{jo} is the nominal parameter, δp_{jc} is the correlated variability that includes wafer-to-wafer, die-to-die, and across-die variability and may be systematically correlated with distance on the wafer or reticle[2]. δp_{ju} is the uncorrelated random variability in the devices on a die, which is a function of the geometry of the device (g). True systematic local layout effects should be included in p_{jo} but are often included in δp_{jc} instead.

2. LITHOGRAPHY CHALLENGES AND THE ALLURE OF REGULARITY

The use of subwavelength lithography to print critical dimensions is resulting in a significant increase in the effects of local layout environment. Resolution enhancement techniques (RET) developed for nominal lithography conditions (at tremendous computational cost) are resulting in complex systematic variability in device (and interconnect) structures. Furthermore, RET techniques are not particularly robust across process windows and are amplifying other sources of lithographic variability, including defocusing, exposure dose, misalignment, lens aberrations, and resist and etch processing. To address these challenges, the use of restrictive design rules (RDR) have been proposed[3]. Typical RDRs may simplify the polysilicon layout to two available pitches. The challenge is what pitches to choose, making design feasible with these restricted pitches, and dealing with the area penalty. The use of even more regular structure[4], gratings with very few pitches on polysilicon, metal-one, and metal-two and contacts on grid, may allow the use of "push" rules that may reduce or eliminate the area penalty traditionally associated with RDRs. This will also allow simple rule-based optical proximity correction (OPC).

3. DEVICE CHARACTERIZATION

As process variability issues affect growing classes of analog and digital circuits and are increasingly influenced by systematic effects, more comprehensive device characterization and modeling are required, to both reduce the magnitude of random

residuals as well as to determine the variables that, if controlled, would reduce systematic variations.

Traditionally, individual devices with pads are characterized on automated wafer steppers. Throughput is low and testing and pad overhead associated with obtaining large number of measurements is high. More recent approaches have tried to improve "silicon density" through ring oscillator (RO) structures[5] and multiplexed transistor arrays[6]. The former allow for relatively simple on-chip characterization of oscillation frequency but "integrate" all the variations in all the devices of the RO into a single measured number significantly reducing information content. Transistor arrays provide high-density access to multiple devices for characterization but have provided slow characterization through off-chip analog measurement with additional complexity in removing the effects of switch resistances[7]. We will discuss more recent work on the design of on-chip current-voltage and capacitance-voltage characterization circuits that allow for the rapid characterization of a large, dense array of multiplexed devices, eliminating the effects of switch resistances and providing digital interfaces.

4. STATISTICAL MODELLING

In analyzing the resulting measurement data, physical modeling allows the correlations between parameters to be immediately known. For example, in understanding the random components of variability, it is recognized that fluctuations in channel length go as $\sigma_L^2 \propto 1/W$ while variations in parameters such as doping density and oxide thickness go as $\sigma_p^2 \propto 1/WL$, where W is the device width and L is the device length. Backward propagation of variances (BPV)[8] allows these variances to be determined from measured model parameters if one knows the equations (physics) behind these parameters. This is straightforward for more "physical" models such as EKV but challenging for the more empirical BSIM models.

If these physical relationships are not known, then principal component analysis[9] can be used to find correlations between model parameters. The problem is that the resulting principal components contain no physical information and complex geometric relationships like $1/\sqrt{W^{n1}L^{n2}}$ are often required to fit the resulting data.

5. DESIGN APPROACHES TO IMPROVE CIRCUIT ROBUSTNESS

Circuit approaches can also be used to reduce the effects of variability. Examples include using gated feedback for latch structures to ensure writeability while preserving noise margins, the use of more latch transparency to provide more forgiving timing budgets, adaptive circuits for clocking[10], leakage control[11], power management[12], and basic SRAM cells with more than six transistors[13].

6. CONCLUSIONS

Addressing yield and variability challenges in deep submicron CMOS requires a combination of design rules, layout regularity, characterization, and modeling. Circuit techniques, combining adaptability with structures that reduce the effects of device strength ratios, can be used to mitigate the impact of variability.

7. REFERENCES

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