Current saturation in zero-bandgap, top-gated graphene field-effect transistors

INANC MERIC[1], MELINDA Y. HAN[2], ANDREA F. YOUNG[3], BARBAROS OZYILMAZ[3†], PHILIP KIM[3] AND KENNETH L. SHEPARD[1*]

[1]Department of Electrical Engineering, Columbia University, New York 10027, USA
[2]Department of Applied Physics and Applied Mathematics, Columbia University, New York 10027, USA
[3]Department of Physics, Columbia University, New York 10027, USA
[†]Present Address: Department of Physics, NUS 2 Science Drive 3, 117542 Singapore
*e-mail: shepard@ee.columbia.edu

Published online: 21 September 2008; doi:10.1038/nnano.2008.268

The novel electronic properties of graphene[1–4], including a linear energy dispersion relation and purely two-dimensional structure, have led to intense research into possible applications of this material in nanoscale devices. Here we report the first observation of saturating transistor characteristics in a graphene field-effect transistor. The saturation velocity depends on the charge-carrier concentration and we attribute this to scattering by interfacial phonons in the SiO_2 layer supporting the graphene channels[5,6]. Unusual features in the current–voltage characteristic are explained by a field-effect model and diffusive carrier transport in the presence of a singular point in the density of states. The electrostatic modulation of the channel through an efficiently coupled top gate yields transconductances as high as 150 μS μm^{-1} despite low on–off current ratios. These results demonstrate the feasibility of two-dimensional graphene devices for analogue and radio-frequency circuit applications without the need for bandgap engineering.

Field-effect transistors based on carbon nanotubes have been the subject of intensive research for the last decade[7–11]. The limited control over the chirality and diameter of nanotubes (and the associated electronic bandgap) remains a major problem. A further limitation is the requirement for sufficiently tightly packed arrays of nanotubes to achieve current levels comparable to silicon field-effect devices[12]. Graphene offers many of the advantages of carbon nanotubes—carrier mobilities of up to 2×10^4 cm^2 V^{-1} s^{-1} in substrate supported devices[2–4] and large ($\sim 1 \times 10^8$ A cm^{-2}) critical current densities[1]—without the need for assembling large parallel arrays of nanotubes to achieve high on currents. The fabrication of the first field-effect graphene-based devices[1] led to an explosion of interest in the electronic properties of graphene. In graphene, the charge carriers in the two-dimensional (2D) channel can change from electrons to holes with the application of an electrostatic gate, with a minimum density (or Dirac) point characterizing the transition. The zero bandgap of graphene limits achievable on–off current ratios (I_{on}/I_{off}). Bandgaps of up to 400 meV have been introduced by patterning graphene into narrow ribbons[13–15], although this has resulted in significant mobility degradation and fabrication challenges. Bandgaps can also be achieved through the application of perpendicular electric fields to bilayer graphene structures[16,17], but these gaps are far less than 400 meV and would lead to significant band-to-band tunnelling.

In this Letter, we describe the design of a top-gated graphene field-effect transistor (GFET) based on a high-κ gate dielectric without bandgap engineering. Despite $I_{on}/I_{off} \approx 7$, high transconductances and current saturation are achieved, making this device well-suited for analogue applications. The GFETs (Fig. 1a) have source and drain regions that are electrostatically doped by the back gate, which enables control over the contact resistance and threshold voltage of the top-gated channel. Figure 1b shows a GFET structure with 3-μm source–drain separation, a 1-μm top-gate length and a device width of 5 μm. We present representative measurement results for a similar device with a width of 2.1 μm. Figure 1c shows source–drain small-signal conductance of $g_{ds} \triangleq (\partial I_d/\partial V_{sd})|_{V_{gs-back}, V_{gs-top}}$ where I_d is the current into the drain and V_{sd} is the source–drain voltage (near $V_{sd} = 0$ V) for varying back-gate ($V_{gs\text{-}back}$) and top-gate ($V_{gs\text{-}top}$) bias. These data are taken at 1.7 K in order to suppress gate hysteresis by freezing out trapped charge, allowing a more accurate estimate of the top-gate capacitance. Room-temperature measurements are presented in the Supplementary Information. The back-gate capacitance (C_{back}) is $\sim$12 nF cm^{-2} (thickness of 285 nm, $\kappa \approx 3.9$). Sheet carrier concentrations (electrons or holes) in the source and drain regions can be approximated by

$$n \cong \sqrt{n_0^2 + (C_{back}(V_{gs-back} - V^0_{gs-back})/e)^2}$$

where $V^0_{gs\text{-}back}$ is the back-gate-to-source voltage at the Dirac point in these regions and n_0 is the minimum sheet carrier concentration as determined by disorder and thermal excitation[18,19]. From the constant top-gate voltage slice of Fig. 1f, $V^0_{gs\text{-}back} \approx 2.7$ V, indicating slight p-type doping, which is most likely due to impurities adsorbed to the graphene. Under the top gate, carrier concentrations are determined by both the front and back gates,

$$n \cong \sqrt{n_0^2 + ([C_{back}(V_{gs-back} - V^0_{gs-back}) + C_{top}(V_{gs-top} - V^0_{gs-top})]/e)^2}$$

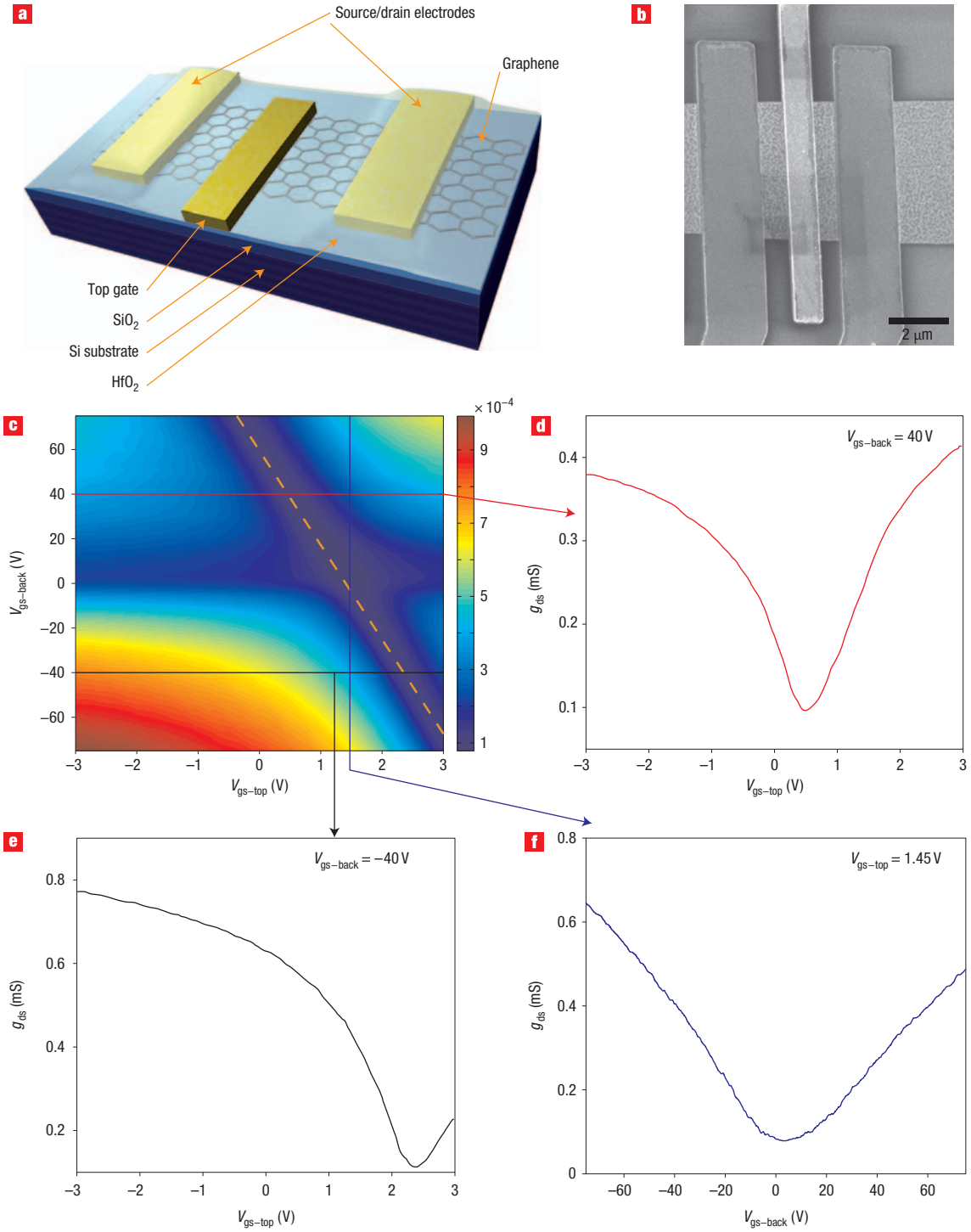

Figure 1 Basic top-gated graphene FET design. a, Schematic of a graphene FET on a Si/SiO_2 substrate with a heavily doped Si wafer acting as a back gate and a gold top gate. **b**, SEM micrograph showing a representative graphene top-gated FET. The top-gate of this device is 1 μm long, with 3 μm spacing between the source–drain contacts. All electrodes are Cr/Au. **c**, Small-signal source–drain conductance (g_{ds}) around $V_{sd} = 0$ V as a function of $V_{gs\text{-}top}$ and $V_{gs\text{-}back}$ at 1.7 K. The dashed line tracks the location of the Dirac point for the top gate with a slope $C_{top}/C_{back} = 46$. **d**, g_{ds} as a function of $V_{gs\text{-}top}$ at $V_{gs\text{-}back} = 40$ V. **e**, g_{ds} as a function of $V_{gs\text{-}top}$ at $V_{gs\text{-}back} = -40$ V. **f**, g_{ds} as a function of $V_{gs\text{-}back}$ at $V_{gs\text{-}top} = 1.45$ V.

with $V^0_{gs\text{-}top} \approx 1.45$ V, where C_{top} is the effective top-gate capacitance per unit area. The slope of the dashed line shown in Fig. 1c, which tracks the location of the Dirac point, has the slope $C_{top}/C_{back} \approx 46$, giving $C_{top} \approx 552$ nF cm^{-2}, more than twice that of previously demonstrated devices[20–23]. If one takes the top-gate capacitance as being the series combination of the electrostatic capacitance (C_e) of the gate dielectric and the quantum capacitance (C_q), then $C_{top} = C_q C_e/(C_q + C_e)$

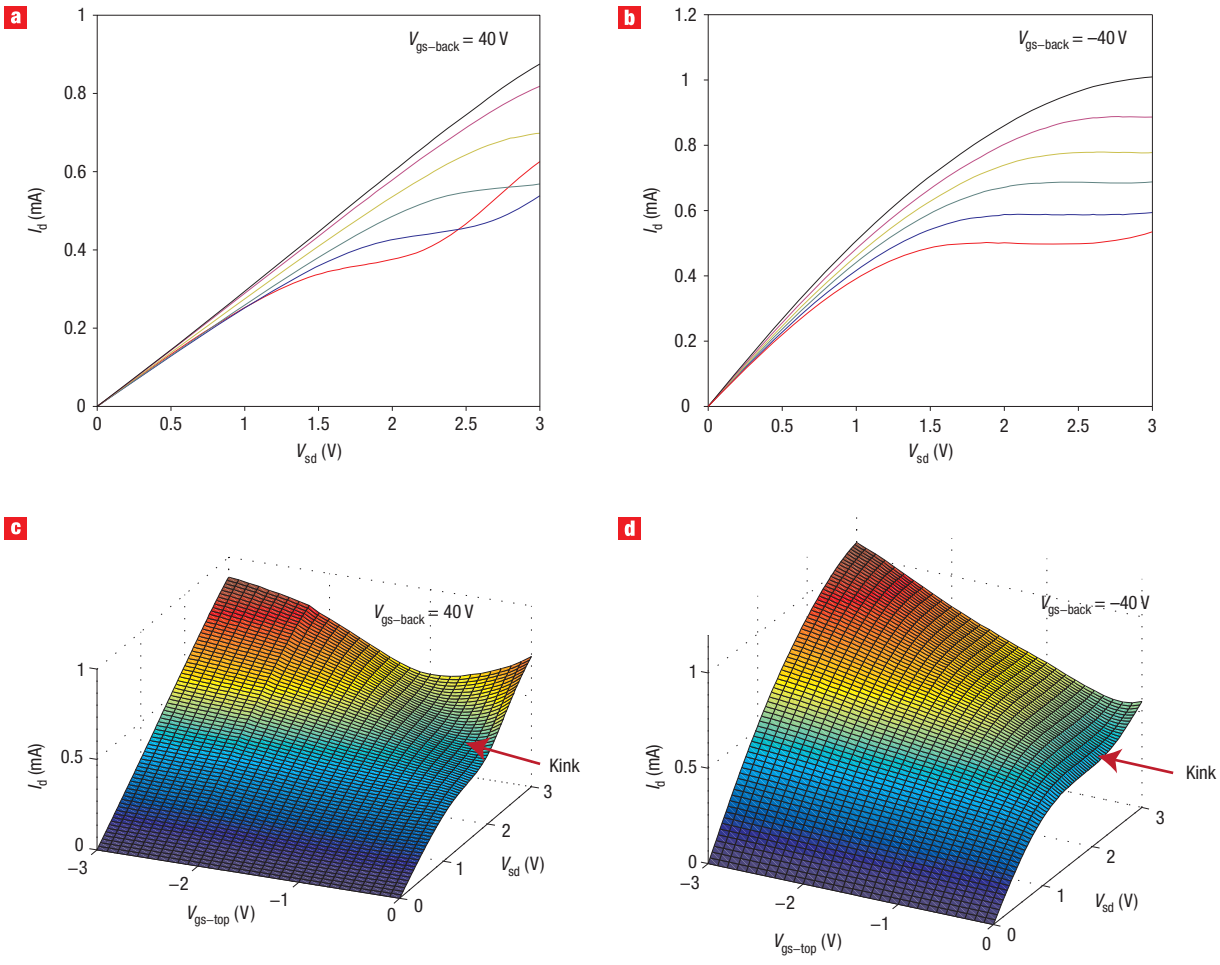

Figure 2 Current–voltage characteristics of the GFET device. a, Drain current (I_d) as a function of source-to-drain voltage (V_{sd}) for $V_{gs\text{-}top} = -0.3$ V, -0.8 V, -1.3 V, -1.8 V, -2.3 V and -2.8 V (from bottom to top) for $V_{gs\text{-}back} = 40$ V. **b**, I_d as a function of V_{sd} for $V_{gs\text{-}top} = -0.3$ V, -0.8 V, -1.3 V, -1.8 V, -2.3 V and -2.8 V (from bottom to top) for $V_{gs\text{-}back} = -40$ V. **c**, Full contour plot of I_d as a function of $V_{gs\text{-}top}$ and V_{sd} at $V_{gs\text{-}back} = 40$ V. The 'kink' produced by the entry of the minimal density point into the channel is marked by a red arrow. **d**, Full contour plot of I_d as a function of $V_{gs\text{-}top}$ and V_{sd} at $V_{gs\text{-}back} = -40$ V.

with $C_q = \sqrt{(n/\pi)} \times e^2/v_F\hbar$, where v_F is the Fermi velocity[24]. For $C_q \approx 2\ \mu F\ cm^{-2}$ for the relevant range of n ($0.5–10 \times 10^{12}\ cm^{-2}$), then $C_e \approx 762$ nF cm^{-2}, which is slightly less than the 944 nF cm^{-2} predicted for the HfO_2 gate insulator (thickness of 15 nm, $\kappa \approx 16$), probably due to surface impurities trapped between the HfO_2 and graphene, increasing the effective gate insulator thickness. Two representative constant back-gate voltage slices at $V_{gs\text{-}back} = 40$ and -40 V are shown in Fig. 1d and e, respectively. The low-field field-effect mobility, $\mu_{FE} = (1/C_{top})(\partial g_{ds}/\partial V_{gs-top})$, of the device is $\sim$1,200 cm^2 V^{-1} s^{-1}; the conductance minimum is $\sim$78.3 $\mu S \approx 2e^2/h$. The conductance shown in Fig. 1d and e saturates for large top-gate voltages due to the series resistance of the source–drain regions. For $V_{gs\text{-}back} = 40$ V, the source and drain regions are n-type with series resistances of $\sim$1.2 kΩ each; for $V_{gs\text{-}back} = -40$ V, the source and drain regions are p-type with series resistances of $\sim$700 Ω each.

All subsequent measurements are shown for ambient conditions. Figure 2a,b shows the measured I_d as a function of V_{sd} (for different $V_{gs\text{-}top}$ voltages) at $V_{gs\text{-}back}$ of 40 and -40 V, respectively. Figure 2c,d shows the complete I_d characteristics as a contour plot in the $V_{gs\text{-}top}$–V_{sd} plane. To understand these curves, we focus first on the I_d curve from Fig. 2a for $V_{gs\text{-}top} = -0.3$ V, which shows a pronounced 'kink' in the characteristic and is shown in more detail in Fig. 3a. Similar to the features observed in ambipolar semiconducting nanotubes FET[25], these kinks in the I_d characteristics signify the presence of an ambipolar channel. The carrier concentration in the channel, shown schematically in Fig. 3b for different points in the I–V trace, is calculated using a field-effect model:

$$n(x) = \sqrt{n_0^2 + (C_{top}(V_{gs-top} - V(x) - V_0)/e)^2}$$

where

$$V_0 \cong V^0_{gs-top} + (C_{back}/C_{top})(V^0_{gs-back} - V_{gs-back})$$

functions as a device threshold voltage, controlled by the back gate; x is the distance along the graphene channel and $V(x)$ is the potential in the channel. For the device in Fig. 3, with channel length L, $V(L) = V_{sd}$, so that for $V_{sd} \leq V_{sd\text{-}kink} \approx V_{gs\text{-}top} - V_0$ current is carried by holes throughout the length of the channel (Fig. 3b, I). The linear relationship between $V_{gs\text{-}top}$ and $V_{sd\text{-}kink}$ is also evident

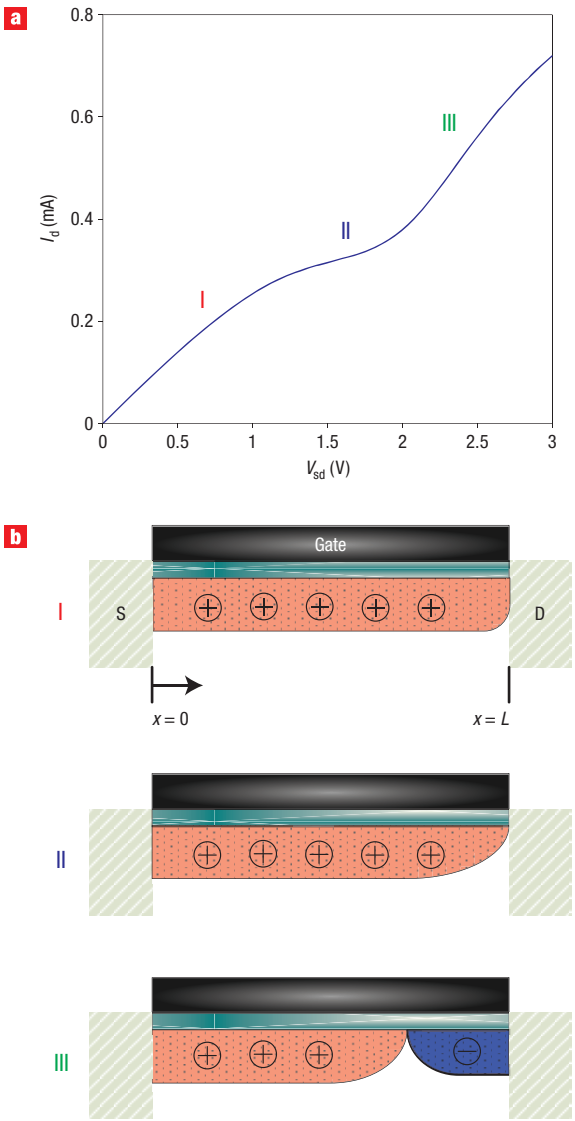

Figure 3 Kink effect in GFET devices. a, Measured $I-V$ characteristic at $V_{gs\text{-}back} = 40$ V and $V_{gs\text{-}top} = -0.3$ V. Three points (I, II and III) are identified in the $I-V$ curve. **b**, Schematic demonstration of the carrier concentration under the top-gated region. At point I ($V_{sd} < V_{sd\text{-}kink}$), the channel charge at the drain end begins to decrease as the minimal density point enters the channel. At point II ($V_{sd} = V_{sd\text{-}kink}$), the minimal density point forms at the drain. For $V_{sd} > V_{sd\text{-}kink}$ (point III), an electron channel forms at the drain.

in the contour plots of Fig. 2c,d. For $V_{sd} = V_{sd\text{-}kink}$, the vanishing carrier density produces a 'pinch-off' region at the drain (Fig. 3b, II) that renders the current in the channel relatively insensitive to V_{sd} and results in the pronounced kink seen in the $I-V$ characteristic. For $V_{sd} > V_{sd\text{-}kink}$, the minimal density point resides in the channel, producing a pinch-off region that moves from source to drain with increasing drain bias magnitude (Fig. 3b, III). In this bias range the carriers in the channel on the source side of the minimal density point are holes, and those on the drain side are electrons. The voltage drop across the 'hole' portion of the channel remains fixed at $V_{sd\text{-}kink}$, while the voltage drop across the 'electron' portion increases as $V_{sd} - V_{sd\text{-}kink}$. In this ambipolar regime, the pinch-off point becomes a place of recombination for holes flowing from the source and electrons flowing from the drain. Because there is no bandgap, no energy is released in this recombination. We note that back-gated GFETs with thick (~300 nm) gate oxides show a decidedly weaker kink effect due to the degraded electrostatics of the device (see Supplementary Information, Fig. S1a). At high values of V_{sd}, these devices become weakly coupled to the gate electrode and show characteristics that resemble punch-through in silicon MOSFETs[26] (see Supplementary Information, Fig. S1b).

For the $I-V$ curves at $V_{gs\text{-}back} = -40$ V and $V_{gs\text{-}top} < -0.8$ V (Fig. 2b), the device shows flat saturating $I-V$ characteristics (high-field regime for a unipolar channel). To accurately model these characteristics, the drift velocity must be assumed to saturate at some value v_{sat} for electric fields beyond a critical electric field (E_{crit}). This is consistent with the carrier drift velocity eventually saturating due to optical-phonon scattering, as in the case of metallic nanotubes[27,28]. For values of $V_{gs\text{-}top}$ that are sufficiently negative, such that $V_{sd\text{-}kink} > E_{crit}L$, the $I-V$ characteristics show a strongly saturating behaviour in the unipolar region, with the kink indicating a transition to an ambipolar channel. Large enough electric fields are reached in the channel at the drain end for the holes to reach saturation velocity, resulting in an I_d that becomes independent of V_{sd}.

With this consideration, the current in the channel is expressed by[29]

$$I_d = \frac{W}{L}\int_0^L en(x)v_{drift}(x)dx$$

where L is the channel length and W is the channel width. Current continuity forces a self-consistent solution for the potential $V(x)$ along the channel. We approximate the carrier drift velocity (v_{drift}) by a velocity saturation model[30]:

$$v_{drift}(x) = \frac{\mu E}{1 + \mu E/v_{sat}}$$

where v_{sat} is the saturation velocity of the carriers. For simplicity, we assume that both electrons and holes are characterized by the same μ and v_{sat} values in our model. A closed-form analytical expression for I_d can be derived from these expressions (see Supplementary Information). Figure 4a shows a comparison of this model with the measured data at $V_{gs\text{-}back} = -40$ V. As input parameters, the fit uses a low-field mobility of 550 $cm^2\,V^{-1}\,s^{-1}$, a minimum sheet carrier density of $0.5 \times 10^{12} cm^{-2}$, and source–drain series resistances of 700 Ω, comparable to those found from the analysis of Fig. 1. For holes v_{sat} is found to vary between 6.3×10^6 cm s^{-1} at high densities (at $n \approx 10 \times 10^{12}$ cm^{-2}) and 5.5×10^7 cm s^{-1} at low densities (near $n = n_0$). This apparent dependence of v_{sat} is clearly demonstrated in Fig. 4b, where we display the v_{sat} obtained from the model fit as a function of E_F modulated by $V_{gs\text{-}top}$. Remarkably, the observed v_{sat} shows a linearly increasing trend with E_F^{-1}. Within the relaxation time approximation to the Boltzmann transport equation, we explain that such a relation is indeed expected for hot carriers in graphene scattered by optical phonons (see Supplementary Information), where we obtain a simple relation $v_{sat} = v_F(\hbar\Omega/E_F)$ with $\hbar\Omega$ designating the relevant optical phonon energy. The solid line in Fig. 4b represents the linear fit to this model, from which we obtained an optical phonon energy of 54 meV. Note that this value is close to the 55 meV surface phonon energy of SiO_2 (refs 5,31) and consistent with the observation of the effect of this phonon energy on temperature-dependent low-field mobility[6]. We also remark that this phonon energy is significantly below the 200 meV longitudinal zone boundary phonon of intrinsic graphene[32], suggesting that the saturation velocity in future

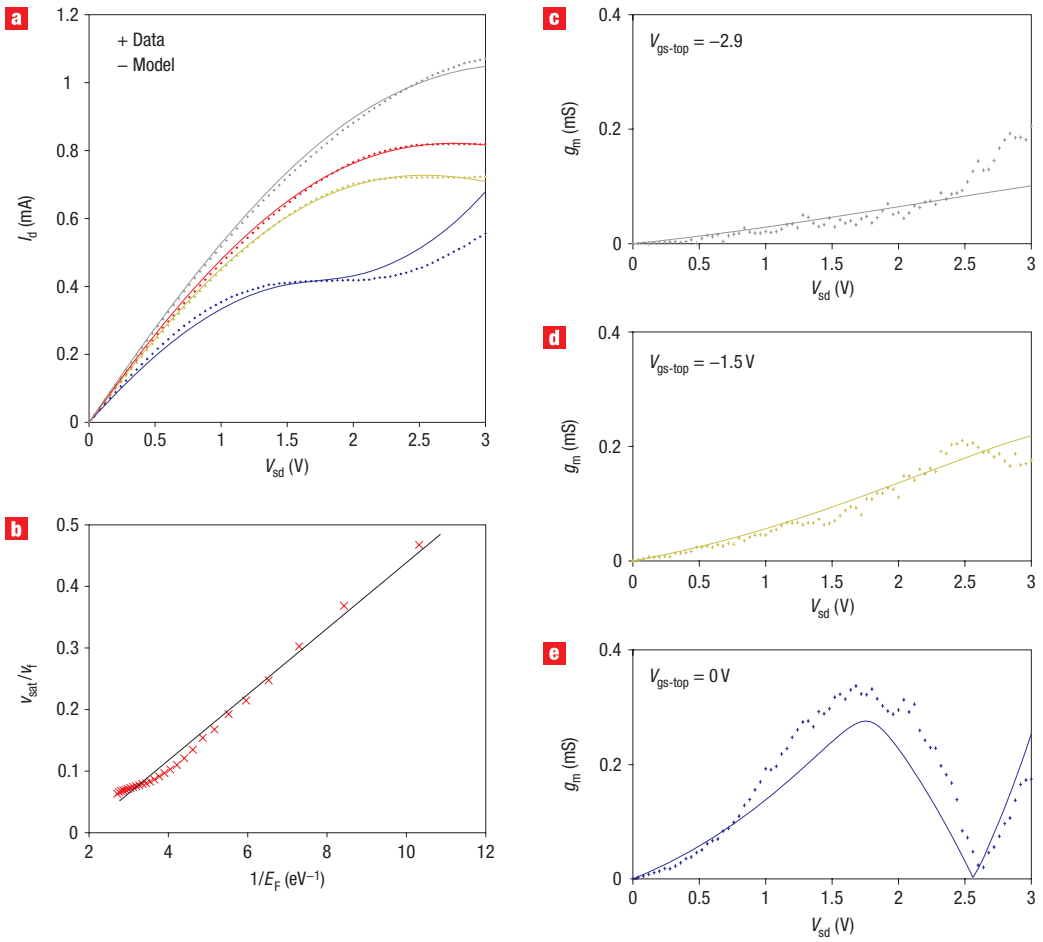

Figure 4 Field-effect modelling of the GFET device. a, Model (solid) and measured (dashed) $I_d - V_{sd}$ curves are compared for $V_{gs\text{-}back} = -40$ V at $V_{gs\text{-}top} = 0$ V, -1.5 V, -1.9 V and -3 V (from the bottom to the top). **b**, Measured density dependence of v_{sat} (red crosses as extracted from the fit). A least-squares fit (solid black line) between E_F values of 0.1 and 0.37 eV determines a slope that corresponds to a phonon energy of 54 meV. A fit that passes through $v_{sat} = 0$ and $1/E_F = 0$ predicts a slightly lower phonon energy. **c–e**, Small-signal transconductance (g_m) as a function of drain-to-source voltage (V_{sd}) for $V_{gs\text{-}top} = -2.9$ V (**c**), $V_{gs\text{-}top} = -1.5$ V (**d**) and $V_{gs\text{-}top} = 0$ V (**e**).

generations of graphene transistors may be augmented by choosing different substrates with higher phonon energies.

Figure 4c–e shows the small-signal device transconductance, $g_m \triangleq (\partial I_d/\partial V_{gs-top})|_{V_{sd},V_{gs-back}}$ as a function of V_{sd} for three different values of $V_{gs\text{-}top}$. Model and measurement show good agreement. The g_m values exceed 320 μS (which is equivalent to a transconductance of ~150 μS per μm) for these 2.1-μm-channel-length devices at $V_{gs\text{-}top} = 0$ V, $V_{gs\text{-}back} = -40$ V and $V_{sd} = 1.6$ V. Removing the effect of series resistance, the device's intrinsic transconductance is ~833 μS μm^{-1} at $v_{sat} = 5.5 \times 10^7$ cm s^{-1}. In comparison, velocity-saturated n-channel 65-nm silicon MOSFETs deliver transconductances of ~1.5 μS μm^{-1} with gate capacitances of ~1.77 μF cm^{-2}. At this gate capacitance, which is close to graphene's quantum capacitance, the graphene transistor would have a transconductance of >2.9 mS μm^{-1}. As expected, and as is evident in Fig. 4e, the transconductance goes to zero at $V_{sd} = V_{sd\text{-}kink}$. The highest transconductances are observed in the unipolar regime away from $V_{sd\text{-}kink}$, which can be achieved by proper choice of V_0. Therefore, the device is most likely to be operated in the high-transconductance, velocity-saturated region with V_{sd} below $V_{sd\text{-}kink}$.

METHODS

TRANSISTOR FABRICATION

The fabrication of our GFETs began with mechanically exfoliated graphene from Kish graphite, as in ref. 1, on a degenerately doped silicon substrate ($\rho = 0.01$ Ω cm) with a 300-nm thermally grown SiO_2 layer (SiTech). Single-layer graphene pieces were identified optically; Raman spectroscopy was used to verify the single graphene sheets (see Supplementary Information, Fig. S2). Strips of graphene with widths between 1 and 5 μm were selected for the device fabrication. Cr/Au (5 nm/90 nm) electrodes were patterned 3 μm apart by standard electron beam lithography followed by metal deposition and lift-off processes to define the source and drain contacts. A low-temperature atomic-layer-deposition (ALD) process was used to directly grow 15-nm HfO_2 onto the graphene sheet as a high-κ gate dielectric for the local top gate. More details about the growth are provided in the Supplementary Information. Top gate electrodes were then fabricated using the same process as above.

DEVICE MEASUREMENT

The low-temperature g_{ds} measurements of Fig. 1 were carried out at 1.7 K (in a pumped helium cryostat) with standard lock-in techniques. The measurements of Figs 2–4 were measured with an Agilent 4155C Semiconductor Parameter Analyzer in a two-probe configuration at room temperature using Cascade DCP-150 probes. The degenerately doped silicon substrate was used as the back gate. Throughout all the measurements, leakage currents from the back and top

gates were recorded. Leakage currents through the HfO_2 top gate were always <0.5 pA μm^{-2} over the full $V_{gs\text{-}top}$ bias range. Measurements were reproducible, although we attribute the slightly negative g_{ds} observed in saturation in Fig. 2b, for example, to residual trapped charge in the ALD oxide.

Received 30 June 2008; accepted 12 August 2008; published 21 September 2008.

References

1. Novoselov, K. S. *et al.* Electric field effect in atomically thin carbon films. *Science* **306,** 666–669 (2004).
2. Novoselov, K. S. *et al.* Two-dimensional gas of massless Dirac fermions in graphene. *Nature* **438,** 197–200 (2005).
3. Zhang, Y., Tan, Y.-W., Stormer, H. L. & Kim, P. Experimental observation of the quantum Hall effect and Berry's phase in graphene. *Nature* **438,** 201–204 (2005).
4. Schedin, F. *et al.* Detection of individual gas molecules adsorbed on graphene. *Nature Mater.* **6,** 652–655 (2007).
5. Fratini, S. & Guinea, F. Substrate-limited electron dynamics in graphene. *Phys. Rev. B* **77,** 195415 (2008).
6. Chen, J.-H. *et al.* Intrinsic and extrinsic performance limits of graphene devices on SiO_2. *Nature Nanotech.* **3,** 206–209 (2008).
7. Javey, A. *et al.* High-κ dielectrics for advanced carbon-nanotube transistors and logic gates. *Nature Mater.* **1,** 241–246 (2002).
8. Javey, A. *et al.* Self-aligned ballistic molecular transistors and electrically parallel nanotube arrays. *Nano Lett.* **4,** 1319–1322 (2004).
9. Klinke, C., Chen, J., Afzali, A. & Avouris, P. Charge transfer induced polarity switching in carbon nanotube transistors. *Nano Lett.* **5,** 555–558 (2005).
10. Kang, S. J. *et al.* High-performance electronics using dense, perfectly aligned arrays of single-walled carbon nanotubes. *Nature Nanotech.* **2,** 230–236 (2007).
11. Avouris, P., Chen, Z. & Perebeinos, V. Carbon-based electronics. *Nature Nanotech.* **2,** 605–615 (2007).
12. Akinwande, D., Close, G. F. & Wong, H. S. P. Analysis of the frequency response of carbon nanotube transistors. *IEEE Trans. Nanotech.* **5,** 599–605 (2006).
13. Han, M. Y., Ozyilmaz, B., Zhang, Y. & Kim, P. Energy band-gap engineering of graphene nanoribbons. *Phys. Rev. Lett.* **98,** 206805 (2007).
14. Chen, Z., Lin, Y. M., Rooks, M. J. & Avouris, P. Graphene nano-ribbon electronics. *Phys. E* **40,** 228–232 (2007).
15. Li, X. *et al.* Chemically derived, ultrasmooth graphene nanoribbon semiconductors. *Science* **319,** 1229–1232 (2008).
16. Ohta, T. *et al.* Controlling the electronic structure of bilayer graphene. *Science* **313,** 951–954 (2006).
17. Oostinga, J. B. *et al.* Gate-induced insulating state in bilayer graphene devices. *Nature Mater.* **7,** 151–157 (2008).
18. Adam, S., Hwang, E. H., Galitski, V. M. & Das Sarma, S. A self-consistent theory for graphene transport. *Proc. Natl Acad. Sci. USA* **104,** 18392–18397 (2007).
19. Martin, J. *et al.* Observation of electron–hole puddles in graphene using a scanning single-electron transistor. *Nature Phys.* **4,** 144–148 (2008).
20. Lemme, M. C., Echtermeyer, T. J., Baus, M. & Kurz, H. A. K. H. A graphene field-effect device. *IEEE Electron. Device Lett.* **28,** 282–284 (2007).
21. Huard, B. *et al.* Transport measurements across a tuneable potential barrier in graphene. *Phys. Rev. Lett.* **98,** 236803 (2007).
22. Williams, J. R., Dicarlo, L. & Marcus, C. M. Quantum Hall effect in a gate-controlled p-n junction of graphene. *Science* **317,** 638–641 (2007).
23. Ozyilmaz, B. *et al.* Electronic transport and quantum Hall effect in bipolar graphene p-n-p junctions. *Phys. Rev. Lett.* **99,** 166804 (2007).
24. Das, A. *et al.* Monitoring dopants by Raman scattering in an electrochemically top-gated graphene transistor. *Nature Nanotech.* **3,** 210–215 (2008).
25. Chen, Y.-F. & Fuhrer, M. S. Electric-field-dependent charge-carrier velocity in semiconducting carbon nanotubes. *Phys. Rev. Lett.* **95,** 236803 (2005).
26. Richman, P. *MOSFETs and integrated circuits* (Wiley, New York, 1973).
27. Yao, Z., Kane, C. L. & Dekker, C. High-field electrical transport in single-wall carbon nanotubes. *Phys. Rev. Lett.* **84,** 2941–2944 (2000).
28. Park, J. Y. *et al.* Electron–phonon scattering in metallic single-walled carbon nanotubes. *Nano Lett.* **4,** 517–520 (2004).
29. Brews, J. A charge-sheet model of the MOSFET. *Solid State Electron.* **21,** 345–355 (1978).
30. Canali, C., Majni, G., Minder, R. & Ottaviani, G. Electron and hole drift velocity measurements in silicon and their empirical relation to electric field and temperature. *IEEE Trans. Electron. Dev.* **22,** 1045–1047 (1975).
31. Fischetti, M. V., Neumayer, D. A. & Cartier, E. A. Effective electron mobility in Si inversion layers in metal-oxide-semiconductor systems with a high-kappa insulator: The role of remote phonon scattering. *J. Appl. Phys.* **90,** 4587–4608 (2001).
32. Ferrari, A. C. *et al.* Raman spectrum of graphene and graphene layers. *Phys. Rev. Lett.* **97,** 187401 (2006).

Supplementary Information accompanies this paper at www.nature.com/naturenanotechnology.

Acknowledgements

We thank N. Baklitskaya for her help with the device fabrication. This work was supported by the Semiconductor Research Corporation Focus Centre Research Program through both the Centre for Circuit and Systems Solutions and the Centre on Functional Engineered Nano Architectonics and the US Office of Naval Research grant no. N000150610138.

Author contributions

I.M. and K.L.S. designed the experiments. I.M. performed the experiments and analysed the data. M.Y.H., A.F.Y. and P.K. assisted with data analysis. B.O. assisted with device fabrication. I.M. and K.L.S. co-wrote the paper. All authors discussed the results and commented on the manuscript.

Author information

Reprints and permission information is available online at http://npg.nature.com/reprintsandpermissions/. Correspondence and requests for materials should be addressed to K.L.S.