Solid-State Nanopores Integrated with Low-Noise Preamplifiers for High-Bandwidth DNA Analysis

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Abstract— **Nanopore sensing platforms have been limited in bandwidth and noise performance by the use of external measurement electronics with significant parasitic impedances. In this work, we describe progress toward integrating detection electronics with solid-state nanopore sensors. This new platform for high-bandwidth single-molecule electrochemical DNA analysis includes a low-noise 8-channel 0.13µm CMOS preamplifier with integrated Ag/AgCl microelectrodes. We also demonstrate monolithic integration of solid-state nanopores in the amplifier chip. This arrangement provides an opportunity to extend the useful bandwidth of nanopore sensors by a factor of ten or more.**

I. INTRODUCTION

Nanopore sensors are single-molecule electrochemical systems in which two electrolyte reservoirs are separated by a membrane containing a single nanoscale pore [1]. By establishing an electrical voltage gradient between the chambers, charged molecules can be induced to pass through the pore, with the presence of a molecule resulting in a transient change in the pore's electrochemical conductance.

Numerous promising examples of nanopore sensors have been published, but as a class of devices they remain severely constrained by noise. In the most common experimental setup, a commercial electrophysiology amplifier is used in voltage-clamp mode to record transient current traces from a nanopore. Due to the high impedance of the sensors, at moderate frequencies an increase in current noise density is seen which derives from parasitic capacitances of the support membrane as well as the amplifier inputs. Tracking the fast kinetics of individual molecules demands a wide signal bandwidth. DNA can pass through a nanopore at speeds greater than one base per microsecond, and whether or not nanopores deliver on their significant promise as a sensing platform will depend on the complementary goals of slowing the molecular kinetics and increasing signal-to-noise ratios. Other sensing modalities are also conceivable, such as monitoring tunneling currents with transverse electrodes; these modalities would likely also benefit from integrated measurement electronics.

In this paper we describe the design and fabrication of a system featuring a current preamplifier with on-die Ag/AgCl microelectrodes, significantly reducing input capacitance which is a key contributor to noise. We describe a "two-chip" solution in which the pore and measurement electronics are on separate adjacent dice and a "one-chip" solution in which the pore is directly integrated on the substrate containing the measurement electronics.

II. SYSTEM DESIGN

A. Noise Analysis

The noise spectrum of nanopore current measurements has several distinct regions, as illustrated in Fig. 1 [3]. At low frequencies, one finds 1/f noise and Johnson noise from the pore conductance. At higher frequencies, the dominant noise source is the interaction between the amplifier's voltage noise and any capacitance present on the input node. In this regime the input-referred noise spectral density scales with $i_n^2 \approx (2\pi f C)^2 * e_n$, where e_n is the equivalent input voltage noise power of the amplifier. The value of C here is the sum of several distinct physical capacitances: the thin membrane in which the nanopore is fabricated acts as a capacitor between the cis and trans reservoirs; stray capacitances can be present in any wiring between the electrodes and the amplifier; and the amplifier itself will have a characteristic capacitance at its input.

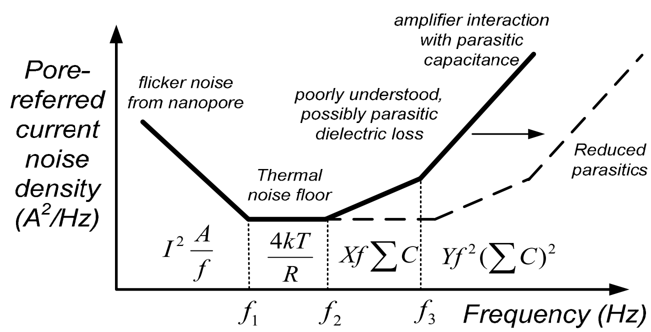

Figure 1. Typical spectral density of nanopore measurement noise

In most recent implementations the membrane capacitance has been the largest of these three elements, contributing as much as several hundred picofarads. It was quickly recognized that noise could be significantly reduced by limiting the fluid contact area with the chip, or by passivating the surface of the chip with a thick dielectric [4]. Membrane capacitance of reported sensors has steadily decreased, and there is reason to have confidence that it can be reduced to the range of 1pF with modern microfabrication techniques.

As the membrane capacitance ($C_{MEMBRANE}$) reduces, noise performance depends more heavily on the reactance of the electrode wiring and amplifier input. Popular electrophysiology amplifiers typically have an input capacitance (C_{IN}) on the order of 15pF, and a wiring capacitance (C_{WIRING}) of several picofarads is not unreasonable. It is clear that the next generation of nanopore sensors will require new amplifiers with wide bandwidth and ultra-low input capacitance if they are to reach their full potential.

B. *Amplifier Circuit Design*

Our custom chip hosts an eight-channel preamplifier with the topology shown in Fig. 2a (and the detailed circuit description of Fig. 2b). Each channel consists of a charge-sensitive preamplifier along with a low-noise transconductance [2] to pass any DC current. The transconductor is wired in a feedback loop which is tuned such that the overall transimpedance gain has a similar first-order response to a classical resistive-feedback stage with a gain of 100MΩ. The attenuator '1/A' is designed as a filter with constant attenuation at signal frequencies but high gain at very low frequencies so that it suppresses DC offsets at the output, improving dynamic range. The frequency response can be tuned by adjusting the loop gain through the gain stage G. Similar to classical high-gain transimpedance amplifiers, the overall response cannot be extended to arbitrarily high frequencies for stability reasons, and a simple filter stage (not shown) is cascaded with the preamplifier output to restore its flat frequency response before being digitized. The value of C_F is programmable as 1pF, 100fF, or 50fF, and the gain-bandwidth product of the OTA is 100MHz. The total input capacitance of each channel is 1pF+C_F.

The 3x3mm die is produced in a standard 0.13µm 1.5V mixed-signal process, with each preamplifier occupying approximately 0.3mm^2 and consuming 5mW.

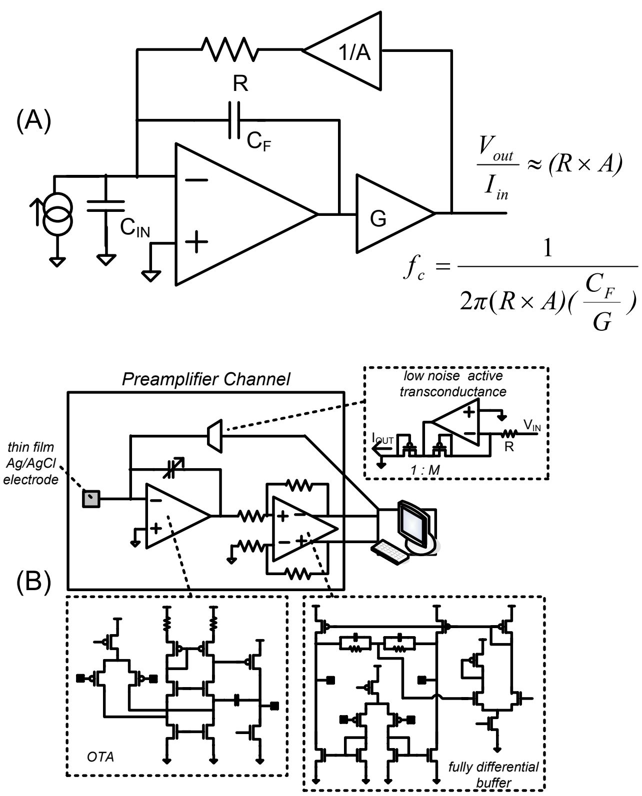

Figure 2. Preamplifier circuit topolgy

III. Fabrication

A. *Ag/AgCl Microelectrodes*

Thin-film Ag/AgCl electrodes [6] are post-fabricated on the surface of the die to enable a direct electrochemical interface between the preamplifier and the electrolyte. In the 0.13µm process used to fabricate the die the top exposed metal is aluminum, which is unsuitable for chemical environments. The aluminum is chemically etched away in phosphoric acid, exposing the adhesion and diffusion barrier layers beneath. Several microns of silver are deposited electrochemically from a plating solution containing aqueous potassium silver cyanide (Transene, Danvers, MA). The surface is then treated with ferric chloride to create a silver chloride coating on the electrode. Images of this fabrication sequence are shown in Fig. 3. This process yields electrodes which are stable operating with nanoampere-scale currents for several hours.

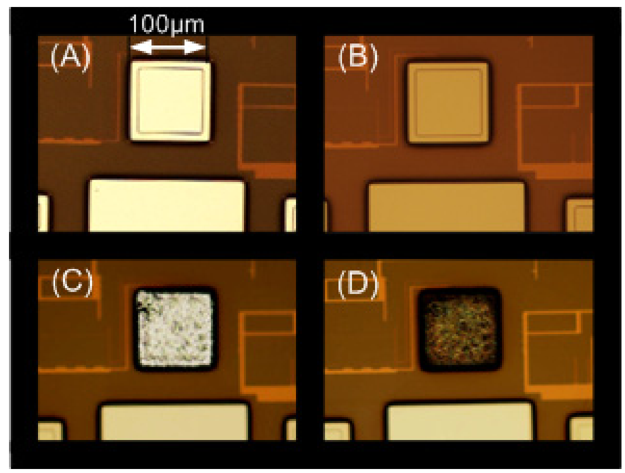

Figure 3. Fabrication of on-chip electrodes. (A) the electrodes as received from the foundry (B) the exposed aluminum is chemically etched away (C) several microns of silver are deposited electrochemically (D) The silver is chlorinated with $FeCl_3$ to create an Ag/AgCl microelectrode.

B. *Two-chip 'stacked' measurement cell*

A custom measurement cell allows us to interface discrete nanopore chips to the integrated preamplifier. As illustrated in Fig. 4, a discrete nanopore chip is mounted in a Teflon fluid cell using KWIK-CAST silicone adhesive (World Precision Instruments, Sarasota, FL), and positioned immediately above the amplifier.

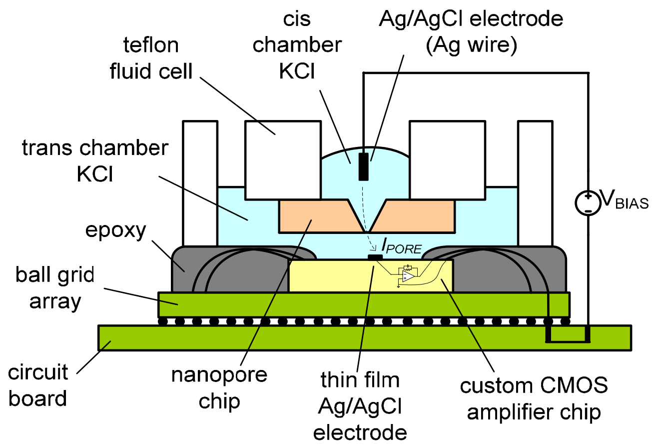

Figure 4. Two-chip 'stacked' measurement cell

In this cell the trans reservoir is in direct contact with the amplifier's microelectrode, while a chlorinated silver wire serves as the cis electrode. Note that since this counterelectrode is only providing a DC voltage bias it is not significantly affected by external wiring parasitics.

C. Single-chip integration

The integration of nanopore sensors with their measurement electronics logically extends itself to monolithic integration of nanopores onto the amplifier die itself. Towards that end, we will discuss a process by which we have post-fabricated solid-state nanopores into the same CMOS preamplifier chip presented here.

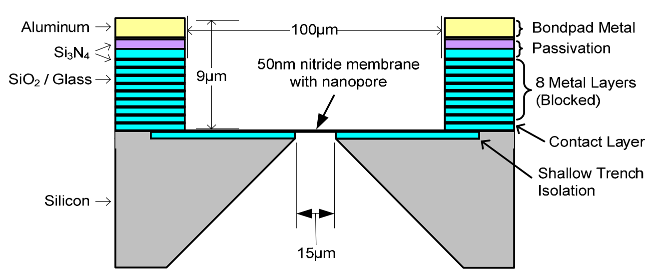

Figure 5. Local cross-section of the post-fabricated silicon nitride membrane

With nanopore post-fabrication in mind, during the design of the chip several 200x200µm areas were reserved for later fabrication of suspended dielectric windows. In these areas of the chip all metal routing layers are blocked, resulting in a thick stack of approximately 8µm of alternating glass fill and silicon nitride capping layers. The majority of the dielectric stack is etched from the front side in an inductively-coupled CHF_3+O_2 plasma, using evaporated chromium as a mask. After depositing and patterning a PECVD Si_3N_4 mask on the back of the die, the chip is mounted in a custom PDMS cell to protect the front side features, and localized openings in the silicon substrate are etched anisotropically in heated 30%wt KOH. A short dip in buffered hydrofluoric acid isolates a single 50nm layer of silicon nitride from the original dielectric stack as a suspended membrane. Finally, nanopores are drilled through these nitride membranes with a high resolution transmission electron microscope [5]. A cross-section of the final window structure is illustrated in Fig. 5, and a TEM image of one of these nanopores can be seen in Fig. 6.

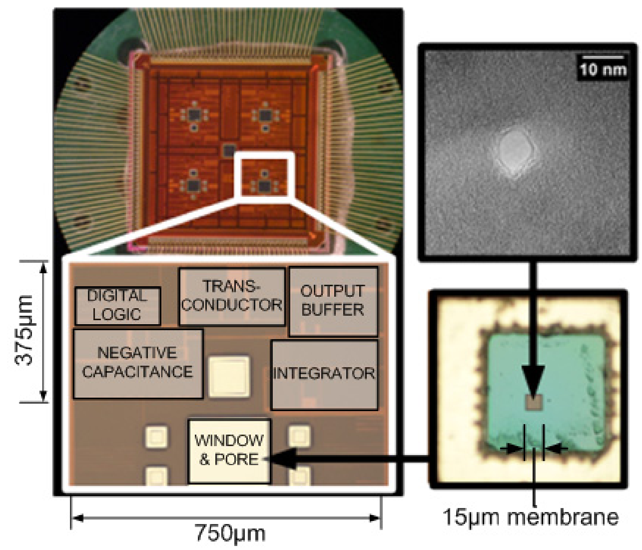

Figure 6. Die photograph showing integrated nanopore. (Insets: layout of one the eight preamplifier channels, an image of a 50nm-thick suspended silicon nitride membrane, and a TEM image of a nanopore drilled in the chip.)

IV. Measurements and Discussion

A. Amplifier Characterization

With no external input, the amplifiers show a measured input-referred noise in good agreement with simulations. Noise spectral density at low frequencies is approximately 12fA/√Hz, comparable to a 110MΩ resistor. At frequencies above 10kHz, the noise is very sensitive to input capacitance, as expected.

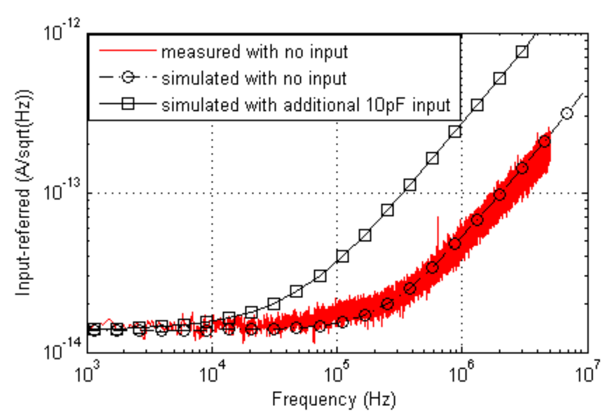

Figure 7. Measured and simulated input-referred noise

B. DNA translocation measurement in the two-chip configuration

As an initial demonstration of the amplifiers and integrated Ag/AgCl electrodes, Fig. 8 shows current blockade events in the two-chip configuration described earlier. Measurements were performed at a bias of 300mV in a potassium chloride buffer (1M KCl, 1mM EDTA, pH 8.0). Lambda DNA (New England BioLabs, Ipswitch, MA) was added to the cis chamber, and the resulting current traces show an appropriate characteristic two-state transient response.

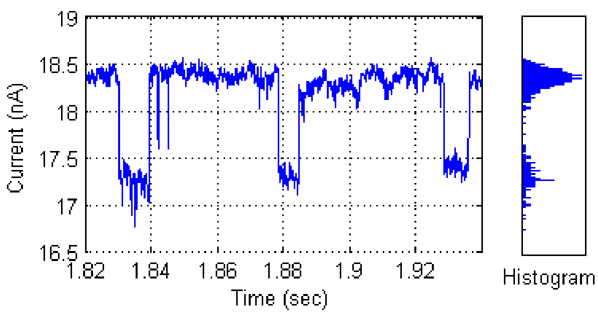

Figure 8. Transient signals of λ-DNA blocking an 8nm silicon nitride nanopore at 300mV bias in 1M KCl.

C. Comparison with existing amplifiers

Today the most popular instrument for nanopore measurements is the Axopatch 200B patch clamp amplifier (Molecular Devices, Sunnyvale, CA). This amplifier has many desirable properties – it is an extremely low-noise instrument which has been optimized for electrophysiology applications that have similar constraints as nanopore sensors. However, as discussed previously, at frequencies above approximately 10kHz the primary factor determining the amplifier noise density is the total input capacitance. On this metric, a discrete amplifier cannot compete with an integrated solution. Additionally, an immediate practical concern is that the Axopatch does not support signal frequencies higher than 100kHz.

Shown in Fig. 9 is a plot of the total RMS current noise that can be expected in several scenarios. The tolerable noise level depends on the signal being measured, but for reasonable solid-state nanopore sensing scenarios we might define the noise-limited bandwidth as the bandwidth at which the noise is larger than $100pA_{rms}$. Scenario A approximates the current state-of-the-art for solid-state nanopores, as measured by a discrete amplifier with C_{IN}=15pF, C_{WIRING}=10pF, and $C_{MEMBRANE}$=60pF. Regardless of noise levels the bandwidth is limited to 100kHz. Scenario B estimates the lowest noise that could likely be achieved with a discrete amplifier by reducing $C_{MEMBRANE}$ to 1pF while C_{IN} and C_{WIRING} remain the same. While this represents a several-fold improvement over today's state of the art, the useful bandwidth is still constrained by wiring and amplifier parasitics. Scenario C simulates the additional benefit of using an integrated amplifier with C_{IN}=1pF and C_{WIRING}=0. Trace D plots the measured input noise floor of our preamplifier, with no pore connected ($C_{MEMBRANE}$=C_{WIRING}=0).

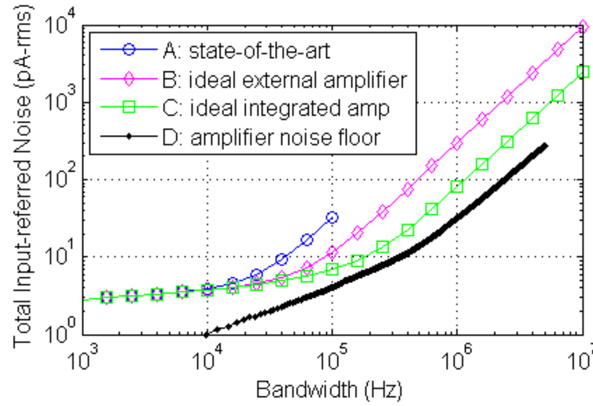

Figure 9. Total solid-state nanopore input-referred RMS currrent noise versus measurement bandwidth for several scenarios as described in the text.

V. Conclusion

We have presented an implementation of an integrated preamplifier for nanopore sensors which significantly reduces electrical parasitics present in measurements with external amplifiers. Moving forward, this arrangement provides an opportunity to extend the useful bandwidth of nanopore sensors beyond 1MHz, as compared to today's limits of sub-100kHz measurements. Such bandwidths are highly relevant to achieve the time resolution necessary for DNA sequencing with nanopores. Additionally, we have described the monolithic integration of solid-state nanopores into a commercial CMOS die. Tight integration of sensors and measurement electronics yields a promising path for the next generation of ultra-sensitive single-molecule biosensing applications.

Acknowledgments

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