NANOPORE DNA SENSORS IN CMOS WITH ON-CHIP LOW-NOISE PREAMPLIFIERS

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ABSTRACT

We present an integrated platform for single-molecule electrochemical analysis in which solid-state nanopore sensors are post-fabricated into a custom CMOS preamplifier die. The usable bandwidth of solid-state nanopore sensors is typically constrained by noise caused by parasitic impedances from the sensor's support substrate and external measurement electronics. By integrating the sensor with a dedicated amplifier we provide a path to significantly reduce these parasitics. The new system includes a low-noise 8-channel preamplifier in a 0.13µm CMOS process. The chip is post-processed to fabricate Ag/AgCl microelectrodes and silicon nitride nanopores.

KEYWORDS

Nanopore, DNA, single-molecule sensors, CMOS

INTRODUCTION

Nanopore sensors are single-molecule electrochemical sensors in which two electrolyte reservoirs are separated by a membrane containing a single nanoscale pore [1]. When a DC voltage is applied between the chambers, it establishes an electrical current corresponding to the transport of dissolved ions through the pore. Local electric fields can also draw charged target molecules, such as DNA, through the pore, resulting in transient changes in the measured ionic current. Nanopores have attracted significant interest in recent years as they are one of few label-free single-molecule sensing techniques. Though nanopores have high hopes as a next-generation DNA sequencing platform, many current research efforts focus on more modest goals such as improving the resolution of measurements and controlling the velocity of molecules passing through a pore.

The first demonstrated sensors utilized transmembrane proteins, which are atomically precise but their lipid bilayer supports can be relatively fragile. Solid-state nanopores can also be etched through dielectric membranes. These pores offer challenges in fabrication and surface chemistry, but also offer the intriguing possibility of integrating nanopores with other nanofabricated devices.

From an instrumentation perspective, nanopores present the challenge of amplifying weak transient signals from very high impedance sources. Typically nanopore sensors are measured using commercially available electrophysiology amplifiers, which are optimized for patch-clamp current measurements of biological systems. Designers of such instrumentation are faced with degrees of compromise between bandwidth, stability, and noise. Capacitance at the input of the amplifier is a primary constraint for all of these metrics. The fast kinetics of single molecules demands wide signal bandwidth, and reaching an acceptable noise level at reasonable bandwidths requires meticulous attention to minimizing stray capacitances. Even so, nanopore sensors remain severely constrained by noise-limited bandwidths of 10-50kHz [2,3].

In this work, we describe the first solid-state nanopore DNA sensors to be monolithically integrated into a standard commercial CMOS process. The sensors are fabricated alongside low-noise current preamplifiers suitable for capturing current signals from these very high impedance sensors. By integrating the sensors on-die we reduce parasitics, achieve a smaller form-factor, and enable nanopore DNA sensors to leverage the fabrication infrastructure of the semiconductor industry.

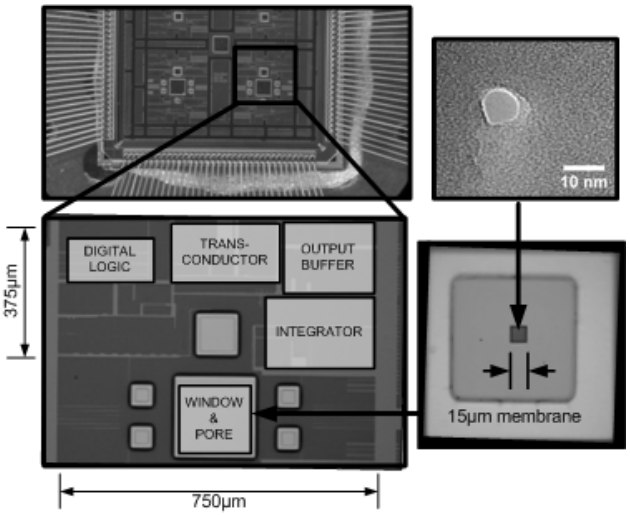

Figure 1:Die photo showing the layout of the preamplifier, post-fabricated silicon nitride membrane, and nanopore.

SYSTEM ANALYSIS

The conductance of a nanopore depends on its geometry and electrolyte conditions, but a typical sensor may present a resistance on the order of 10MΩ to 100MΩ, and be operated with a DC bias of 0.1-0.5V. In a strong electrolyte, molecules passing through the pore result in a transient decrease in conductivity. The duration of these events can range from milliseconds to microseconds

Nanopore measurements have several unique contributions to the noise spectrum, illustrated in Fig. 2 [2]. At low frequencies one finds flicker noise and Johnson thermal noise from the nanopore's ionic

conductance. At high frequencies, the dominant noise source is the interaction between the amplifier's voltage noise and any capacitance at the input. Since nanopores produce transient time-domain measurements, the relevant noise specification is the integrated RMS noise power. This makes the increasing noise density at high frequencies particularly restrictive.

The thin membrane which supports the sensor results in a shunt capacitance between the two electrolyte reservoirs. Since a DC voltage is enforced across the sensor, this capacitance appears in parallel with any capacitance at the input node. In early examples of nanopore sensors this membrane capacitance was more than 300pF, but it is now more commonly in the range of 25pF, and modern microfabrication techniques offer straightforward methods to reduce it to less than 1pF [4].

As the membrane capacitance decreases, it becomes more pressing to reduce any stray parasitics related to wiring and amplifier inputs. Typical patch-clamp amplifiers have input capacitances on the order of 15pF [5].

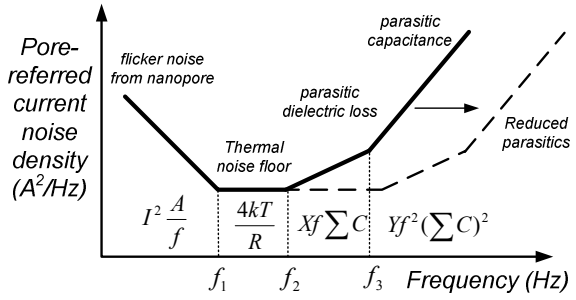

Figure 2: Typical noise regimes in nanopore measurements

PREAMPLIFIER DESIGN

The topology of the custom preamplifier is a variant of the classic transimpedance amplifier. A charge-sensitive integrator is used in conjunction with a feedback loop featuring an active transconductance in the place of a passive feedback resistor. Fig. 3 shows a simplified schematic. The input integrator uses a folded-cascode OTA with a gain-bandwidth product of 100MHz. The feedback transconductor takes advantage of matched PMOS transistors to form a very low-noise current divider [6]. A load-compensated fully-differential buffer drives the output from the chip.

The overall closed-loop response of the system has the familiar shape of a flat low-frequency response followed by a single pole. A filter with an appropriately placed zero is cascaded with the output to cancel the pole and restore a flat frequency response before the signal is digitized. The result is a two-stage transimpedance amplifier with a gain of 106MΩ which operates from DC to frequencies greater than 1MHz. The pole-zero pair is at 25kHz. The total input capacitance of the amplifier is less than 2pF.

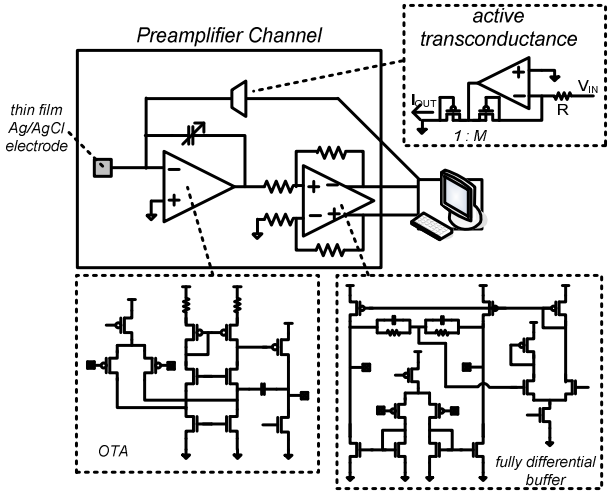

Figure 3: Preamplifier circuit topology.

The 3mm-by-3mm die is produced in a standard 0.13µm 1.5V mixed-signal process. It hosts eight identical preamplifier channels, with each channel occupying approximately 0.3mm^2 and consuming 5mW. A photograph of the die can be seen in Fig. 1.

POST-FABRICATION

Ag/AgCl Microelectrodes

Thin-film Ag/AgCl electrodes [8] are post-fabricated on the surface of the die to avoid packaging parasitics and allow a direct electrochemical interface between the amplifiers and the electrolyte. After etching the standard aluminum contacts from the designated electrodes, several microns of silver are deposited electrochemically from aqueous potassium silver cyanide, and the surface of the silver is then chemically chlorinated with ferric chloride. Images of this sequence are shown in Fig. 4. A key limitation to using microelectrodes is the solubility of AgCl in water, which limits the lifetime of the electrodes. However, our experiments have shown these electrodes to be stable for several hours exposed to 200µL of buffer.

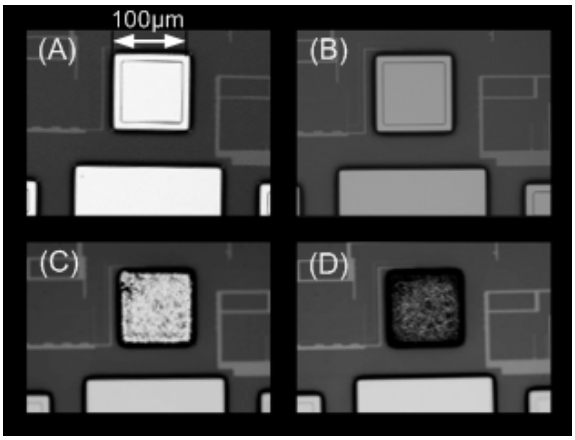

Figure 4: Fabrication of thin-film Ag/AgCl microelectrodes.(A) an aluminum electrode (B) the aluminum is chemically etched (C) silver is electroplated (D) the surface is chemically chlorinated to form an Ag/AgCl electrode

Silicon Nitride Membranes

In the integrated circuit design, several areas are reserved for post-fabricating thin suspended membranes. In these areas all metals have been blocked, leaving an 8μm stack of dielectrics from planarization of the chip's interconnect layers. This stack consists of alternating layers of glass fill and silicon nitride capping layers. The membrane fabrication procedure consists of steps to etch away most of the dielectric stack from the top side as well as remove the silicon substrate from the back side, isolating one Si_3N_4 layer as a thin suspended membrane. A cross-section of the final micromachined structure is illustrated in Fig. 5.

First, a layer of chromium is thermally evaporated onto the top of the chip. Local openings are patterned in the chromium with UV photolithography, and in these areas the majority of the dielectric stack is etched using an inductively-coupled CHF_3+O_2 plasma.

Working from the back side of the die, a film of PECVD Si_3N_4 is deposited and square openings are patterned in the nitride, aligned with the desired window areas on the top side of the chip. The die is mounted in a custom PDMS single-sided etching cell, and the silicon substrate is etched using a heated KOH solution. The chip is manufactured on a <100> p-type wafer, and the KOH etch results in an inverted pyramid cavity whose sidewalls are <111> planes. The etch terminates when it reaches the dielectrics on the top side of the chip.

The removal of the silicon substrate results in a small (15x15μm) suspended dielectric membrane consisting of the bottom few layers of the interconnect passivation, which due to the top-side plasma etch is now a three-level stack of SiO_2-Si_3N_4-SiO_2. A short dip in buffered hydrofluoric acid is used to remove the SiO_2 from both sides and release a single 50nm Si_3N_4 layer as a suspended membrane.

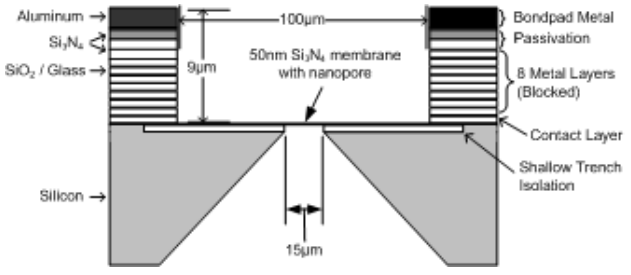

Figure 5: Illustrated cross-section of the final microfabricated silicon nitride membrane.

Solid-State Nanopores

Currently one of the more common methods for fabricating solid-state nanopores is to drill pores with an electron beam via ablation of a thin membrane in a field-emission transmission electron microscope [7]. This method is capable of forming extremely small isolated pores, and allows immediate imaging of the results.

Using this technique, nanopores were drilled into the 50nm on-chip membranes using an HR-TEM at 200kV. Fig. 6 shows a selection of several of these pores. The minimum pore size was approximately 6nm in diameter, which was constrained by the thickness of the membrane; the electron beam focus limits the aspect ratio and pore precision. Typically smaller pores are enabled by membranes which are 25nm or thinner.

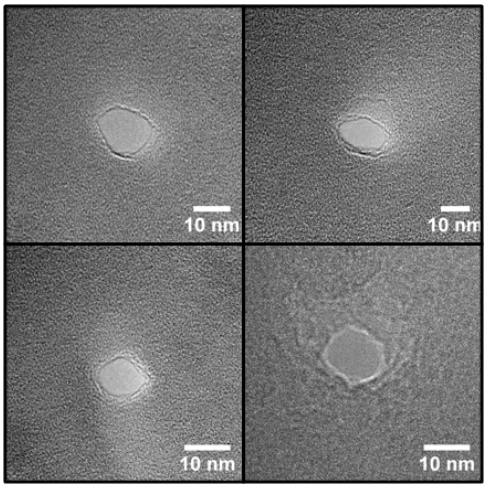

Figure 6: TEM images of several nanopores drilled in the on-chip silicon nitride membranes.

MEASUREMENTS

Preamplifier Characterization

The amplifier noise floor is characterized by measuring its output with no input connected, and dividing by the gain. The measured amplifier noise floor is consistent with simulations, as shown in Fig. 7. With an input-referred noise level of 12fA/√Hz, the preamplifier has a minimum current noise density comparable to a 110MΩ resistor. This noise is due to thermal noise in the feedback transconductor, and does not actually scale with the gain. At high frequencies, the noise density increases as a function of the amplifier's voltage noise applied across the input capacitance.

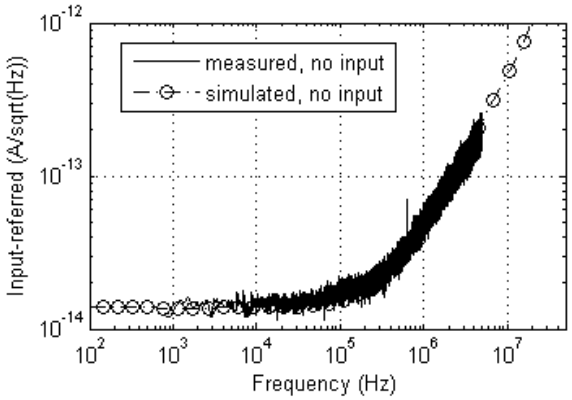

Figure 7: Measured and simulated input-referred noise floor.

DNA Translocation Measurements

As a demonstration of the amplifiers, we have measured DNA translocation events using one of the preamplifer channels and its integrated Ag/AgCl electrode, as shown in Fig. 8. The surface of the chip was exposed to a solution of 1M KCl pH 8.0 and an external Si_3N_4 membrane with a 6nm nanopore was suspended above the chip. A second KCl reservoir was formed above the nanopore chip. λ-DNA was added to one of the reservoirs, and a bias of 300mV was applied between the integrated Ag/AgCl input electrode and a second electrode in the opposite reservoir.. The current traces show a characteristic two-level response.

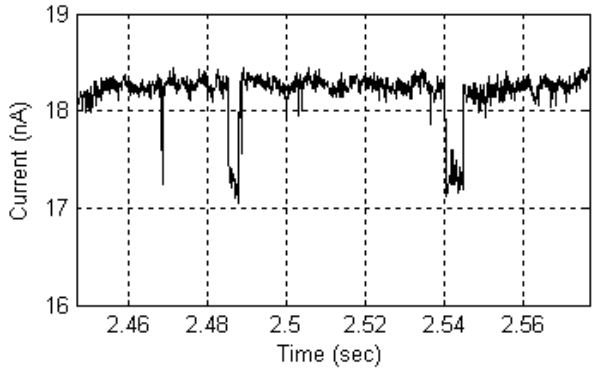

Figure 8: Transient measurement of λ-DNA blockades of a solid-state nanopore.

CONCLUSION

We have presented a low-noise preamplifier with monolithically integrated Ag/AgCl electrodes and solid-state nanopores. This arrangement reduces parasitic impedances associated with external measurement electronics, which are a significant source of noise at high frequencies. Physical integration of nanopores and integrated circuits may provide a natural platform for arrays of nanopore sensors enabling extremely high-throughput single-molecule sensing applications.

ACKNOWLEDGEMENTS

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