GaN Devices on a 200 mm Si Platform Targeting Heterogeneous Integration

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***Abstract*— GaN-based high electron mobility transistors (HEMTs) were fabricated on 200-mm silicon-on-insulator (SOI) substrates possessing multiple crystal orientations. These SOI substrates have the Si (100)-SiO_2-Si (111) structure, which allows Si (111) to be exposed below the buried oxide to enable GaN epitaxial growth adjacent to Si (100). The current collapse in GaN HEMTs of < 150 × 150 μm^2 patterns is 2%–6%, which is remarkably lower than the devices on blanket materials. We believe that stress relaxation resulting from substrate patterning contributes to the reduction of current collapse. By creating small GaN patterns on a larger diameter Si wafer, co-integration of GaN with Si technology may be possible.**

***Index Terms*— GaN, CMOS, Si, metalorganic chemical vapor phase deposition (MOCVD), high electron mobility transistor (HEMT).**

I. Introduction

OVER the past decade, power electronics and radio frequency (RF) communication industries have shown an increased interest in gallium nitride (GaN) due to its superior material and electrical characteristics compared to Si. GaN devices offer high breakdown voltage, low on-state resistance, and excellent high frequency operation that can dramatically improve the performance of RF products [1], [2]. The conventional silicon-based RF devices have a cut-off frequency (f_T) of 445 GHz and have been fabricated using 32 nm Si complementary metal oxide semiconductor (CMOS) technology (L_{GATE} = 28 nm) and it is expected that this f_T will further increase with continued scaling [3]. Despite the impressive f_T numbers, silicon CMOS is not compatible with high-voltage or high-power-density applications, such as those for photovoltaic inverters, electric vehicle charging, and DC power transmission. Because GaN is better suited for these applications, co-integration of GaN with Si may provide a pathway for both high power and high performance applications on a single chip. Various co-integration schemes have already been explored including those by direct bonding [4] and heteroepitaxy [5]. However, high stress during blanket GaN growth on Si limits the wafer diameter due to excessive bowing.

In this letter, we describe a GaN-on-Si co-integration approach using patterned structures which permits the use of 200 mm or larger diameter substrates. Details of substrate preparation, metalorganic chemical vapor phase deposition (MOCVD) epitaxial growth in patterned regions, and fabrication of HEMT devices are discussed. It is shown that the electrical characteristics of co-integrated GaN HEMTs are equivalent to those obtained from GaN on blanket silicon substrate.

II. Experimental Procedure

Hybrid oriented SOI substrates with 80 nm Si (100)/145 nm buried oxide/750 μm Si (111) were used in this study to permit epitaxial growth of hexagonal GaN on the exposed (111) surface regions while permitting Si CMOS fabrication on the (100) surface. The thickness of top Si (100) layer was adjusted to 40 nm by thermal oxidation to meet the requirement of the state-of-the-art 14 nm CMOS technology node.

Patterned regions of various dimensions, ranging from 50 × 50 μm^2 to 200 × 200 μm^2 were created in the SOI substrate by reactive ion etching (RIE) to expose Si (111) below the buried oxide layer to permit selective GaN growth (Fig. 1). The percentage of surface area covered by GaN was nominally 35%, 37%, 39% and 41% for 50 × 50 μm^2, 100 × 100 μm^2, 150 × 150 μm^2 and 200 × 200 μm^2 windows, respectively. We limit the total GaN coverage to less than 50% to maintain the bow and warp within the Si CMOS specification. Si_3N_4 spacers on the sidewalls of the patterned regions were formed to allow electrical isolation between neighboring Si and GaN devices. Additionally, these spacers provide: (i) growth selectivity, and (ii) a barrier to inter diffusion of Si and Ga into neighboring GaN and Si regions, respectively, during the GaN growth. GaN growth was performed on both patterned

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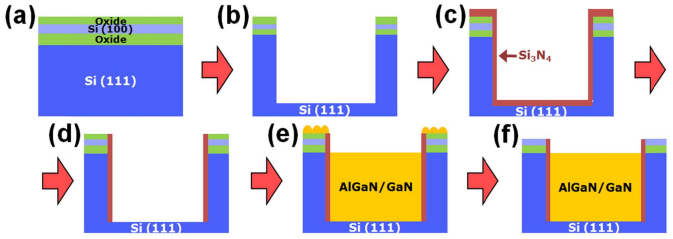

Fig. 1. Hybrid-oriented SOI substrate with top Si (100) and bottom Si (111) preparation for MOCVD growth: (a) CVD-SiO_2 growth, (b) Dry etching to expose Si (111) plane, (c) Si_3N_4 growth via CVD as an isolation and diffusion barrier, (d) Si_3N_4 removal via dry etch to expose Si (111) plane, (e) AlGaN/GaN HEMT growth, (f) CVD-SiO_2 removal via chemical-mechanical planarization.

hybrid SOI and blanket Si (111) substrates in a Veeco's commercial MOCVD reactor operated at 75 torr with high purity trimethylaluminum (TMAl), trimethylgallium (TMGa) and ammonia (NH_3) precursors. Growth parameters were optimized to reduce wafer bow below 50 μm required for Si CMOS processing. The substrate underwent a pre-bake in H_2 at 1050 °C for 1.5 minutes prior to the growth of an AlN nucleation layer (130 nm) and 1.5 μm of GaN growth at 1035 °C. Post growth ramp down occurred at 985 °C to facilitate unintentional carbon doping in GaN. The HEMT structure subsequently grown on the GaN contained a 1 nm AlN spacer, 20 nm $Al_{0.25}Ga_{0.75}N$, and a 3 nm GaN cap layer.

The GaN thickness measured on the Si (111) control wafer was 0.6 μm, and was less than half of that measured on the patterned GaN (1.5 μm) due to micro-loading effects. Electron mobility, drain current, breakdown voltage, and static and pulsed I-V curves were used to study the reliability and performance of these HEMT devices. The direct-current measurements were taken with an Agilent 4155C analyzer. The breakdown voltage measurement was performed by turning the device off (with $V_{GS} = -4$ V) and the V_{DS} is ramped up until the off-state I_{DS} leakage reaches 1 mA/mm. The pulsed I-V measurement was performed by biasing the device at the high voltage off-state quiescent point for 99.9% of the pulse width, then measuring the on-state current at different V_{DS} points for the remaining 0.1% of the pulse width. All the devices measured in this study are passivated with 100 nm of SiN.

III. Results and Discussion

Figures 2 (a) and 2 (b) show a fully processed 200 mm hybrid SOI wafer and an optical micrograph of individual AlGaN/GaN HEMT devices, respectively. The tested devices have $L_{GS} = 3$ μm, $L_G = 3$ μm and $L_{GD} = 3$ μm. Standard device processing steps were used to fabricate the HEMTs.

The cross-sectional scanning electron microscopy (SEM) image of a typical patterned window (before removing the surface SiO_2) in Fig. 3 (a) demonstrates planar epitaxial growth of a 1.5 μm AlGaN/GaN film using an optimized growth process. The patterned region is filled with the HEMT structure with uniform thickness across the wafer. The root-mean-square (RMS) surface roughness of $\sim$ 0.17 nm is obtained using atomic force microscopy (AFM) (Fig. 3 (b)). When the HEMT structure thickness exceeded 1.5 μm,

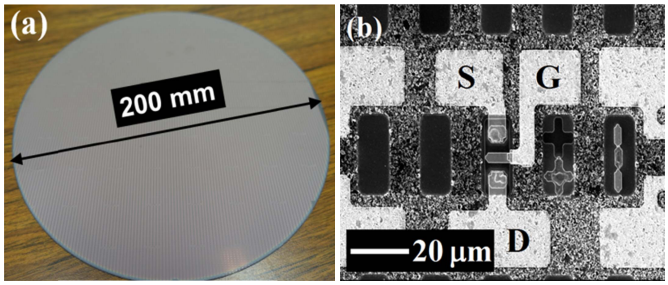

Fig. 2. (a) A 200 mm GaN on Si wafer with (b) AlGaN/GaN HEMTs fabricated in the patterned areas.

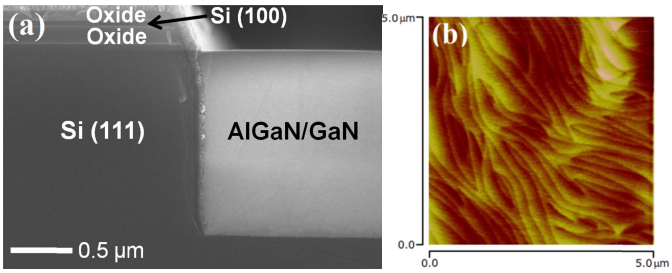

Fig. 3. (a) SEM cross-section of AlGaN/GaN epitaxial growth of 1.5 μm in the window and (b) AFM surface image (5 × 5 μm^2) of AlGaN/GaN epitaxial layer.

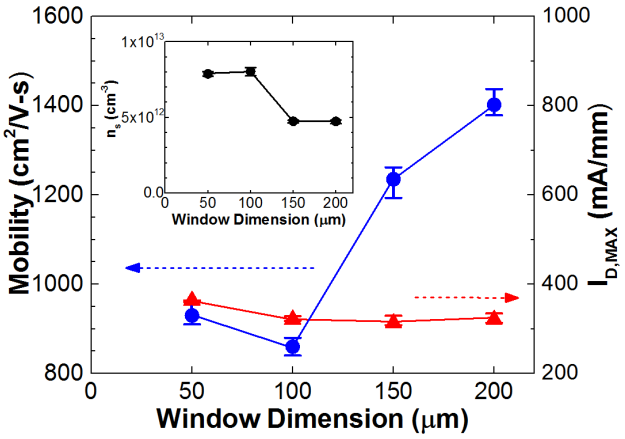

Fig. 4. The electron mobility and the drain current of GaN HEMTs from various window dimensions. Inset shows corresponding carrier density (n_S) as a function of window dimension.

micro-cracks were observed within the GaN windows due to the high tensile stress.

The extracted electron mobility and measured drain current in patterned GaN HEMTs as a function of window dimensions are shown in Fig. 4. The error bars represent the standard deviation from the measurements. The electron mobility of blanket GaN/Si (111) is 1870 cm^2/V-s, and declines with decreasing window dimension. However, these devices show remarkably similar maximum current across different window dimensions. The mobility in GaN HEMTs is known to be highly dependent on tensile strain [6], [7] in the structure; with higher strain leading to higher direct-current (DC) performance. During the epitaxial growth, GaN on blanket Si (111) shows high tensile strain due to thermal mismatch. The decline in electron mobility with decreasing window dimension is believed to be related to higher strain relaxation in smaller windows. Despite the fact that the mobilities are lower than those obtained from

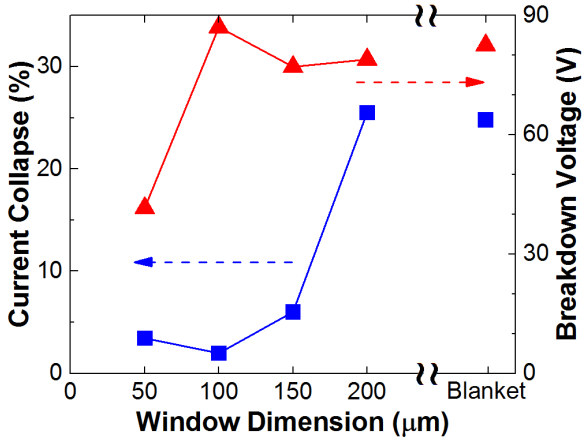

Fig. 5. Current collapse and breakdown voltage of HEMTs are a function of GaN window dimension.

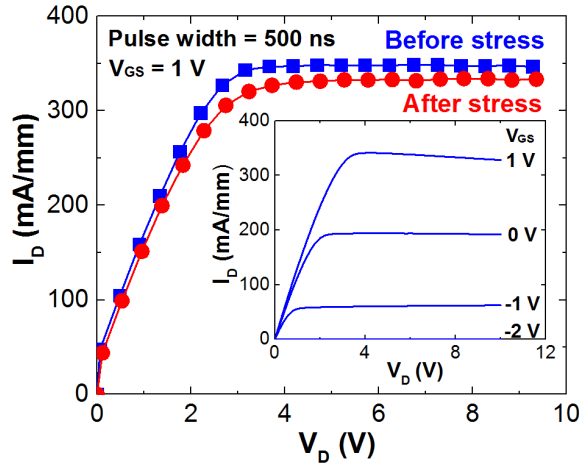

Fig. 6. I-V curves before and after bias stress for GaN HEMTs in 100 × 100 μm^2 window. Inset shows the I_D-V_D plot measured from the same device.

the HEMTs grown on blanket Si (111), the patterned growth can relive the strain without forming cracks in the epitaxial films, which is crucial to wafer-level integration. The inset in Fig. 4 shows carrier density (n_s) as a function of window dimensions, and it shows expected inverse relationship with mobility.

The red curve in Fig. 5 shows the breakdown voltage of HEMTs as a function of the window size. The lower breakdown voltage of 50 × 50 μm^2 windows could be attributed to defects at the GaN/sidewall interface. The blue curve plots current collapse as a function of window size which clearly shows dramatic improvement in current collapse for windows $< 200 \times 200$ μm^2. The current collapse essentially represents the dispersion in device current between the I-V curves before and after bias stress. Minimizing this collapse is one of the major challenges for GaN RF power applications [8]. To measure the current collapse, a pulse width of 500 ns is applied to the patterned GaN HEMTs with the quiescent point of $V_{GS} = -3$ V, $V_{DS} = 10$ V. Figure 6 shows the I_D-V_D curves, before and after bias stress, from devices on 100 × 100 μm^2 window, which correspond to the best current collapse less than 2%. Moreover, the current collapse increases somewhat rapidly to 25.5% for 200 × 200 μm^2 before saturating to the typical bulk GaN value of 25%. The current collapse appears to correlate with the strain relaxation in patterned GaN, which is lower in smaller windows [7]. Although the exact mechanism for this phenomenon needs further investigation, we believe that an interplay between defects and strain in patterned GaN dictates the observed current collapse behavior [9].

IV. Conclusion

In conclusion, a method for co-integrating GaN and Si has been described that may permit fabrication in a conventional CMOS process flow using large area substrates. The patterned GaN HEMTs described above demonstrate comparable electrical characteristics compared to those of conventional blanket GaN HEMTs grown on Si, as well as a reduction in current collapse. Despite the reduction of electron mobility in 100 × 100 μm^2 and smaller windows, a pronounced improvement in the current collapse is observed. Small patterns were used to reduce strain, and therefore improve GaN device performance in the 200 mm Si platform. The size dependence observed confirms the validity of this approach. The need for large-periphery high power devices can potentially be achieved by combining multiple small patterned GaN devices. Once this approach is successful, this technology can extend the GaN-on-Si co-integration platform to high power applications.

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