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CMOS-Integrated Low-Noise Junction Field-Effect Transistors for Bioelectronic Applications

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***Abstract*—In this work, we present a CMOS-integrated low-noise junction field-effect transistor (JFET) developed in a standard 0.18 µm CMOS process. These JFETs reduce input-referred flicker noise power by more than a factor of 10 when compared to equally sized n-channel MOS devices by eliminating oxide interfaces in contact with the channel. We show that this improvement in device performance translates into a factor-of-10 reduction in the input-referred noise of integrated CMOS operational amplifiers when JFET devices are used at the input, significant for many applications in bioelectronics.**

***Index Terms*—1/f noise, JFET circuits, biopotential amplifiers, electrophysiology.**

I. Introduction

LOW-NOISE operational amplifiers are an important tool in the life sciences [1]. Some applications of low-noise amplifiers in biology include extracellular and intracellular electrophysiology [2], [3] and the study of conductance-based sensors such as nanopores [4], [5] and functionalized carbon nanotubes [6]. Low-noise front-ends often consist of an operational transconductance amplifier (OTA) configured as either a transimpedance or voltage amplifier. While these front-ends often take the form of rack-mounted instruments, there is increasing interest in CMOS implementations of these electronics to enable closer integration of the sensor and amplifier with the target biochemical or biological system [1].

In commercial low-noise amplifiers, large discrete JFET devices are often used in the input stages due to their superior flicker noise performance [7]. JFET devices, however, are usually not available in CMOS processes, and low-noise CMOS-integrated OTAs generally cannot take advantage of this benefit. Mitigating the flicker noise introduced by the NFET or PFET devices employed by CMOS OTAs instead is possible by increasing input device size, but this results in additional circuit area, power consumption, and input capacitance. This larger device input capacitance degrades the high frequency noise performance of transimpedance amplifiers. In voltage amplifiers, a large input capacitance increases the voltage division of the input signal.

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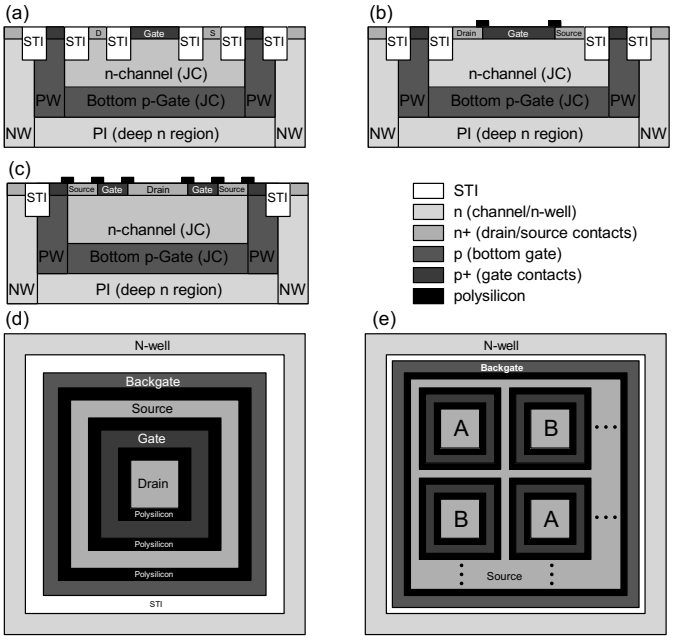

Fig. 1. (a) Device structure of JFETJC n-channel JFET in CMOS. (b) Device structure of JFETLN transistor with polysilicon (PC, black) blocking layer. (c) Cross section view of waffle JFETLN. (d) Top view of waffle JFETLN. (e) Top view of waffle JFETLN differential pair.

Many of these observations have been made in studies based on BiCMOS [8], [9] or CMOS [10], [11] processes with many implants available to form JFET structures. Often for more aggressive CMOS nodes, only a few implants are available to define JFETs. Additionally, shallow-trench isolation (STI) is used for these JFETs to achieve high breakdown voltages [12]. However, this can compromise flicker noise performance because of charge traps at these STI interfaces. Thus, many CMOS-integrated JFETs do not provide significant benefits in low-noise measurement applications.

In this work, we have exploited a 0.18 µm CMOS technology supporting an STI-isolated n-channel JFET device to create a low-noise JFET with no changes to existing mask layer definitions. The original n-type JFET design (JFETJC, Fig. 1a) utilizes the standard CMOS triple-well implants to isolate the bottom gate from the substrate. Two additional mask levels are used for the device (PI, which defines the bottom n-well isolation, and JC, which defines the JFET channel and p-type bottom gate). The JFETJC was optimized for high-voltage and RF operation and has STI in direct contact with the channel of the device [12]. As a result, the

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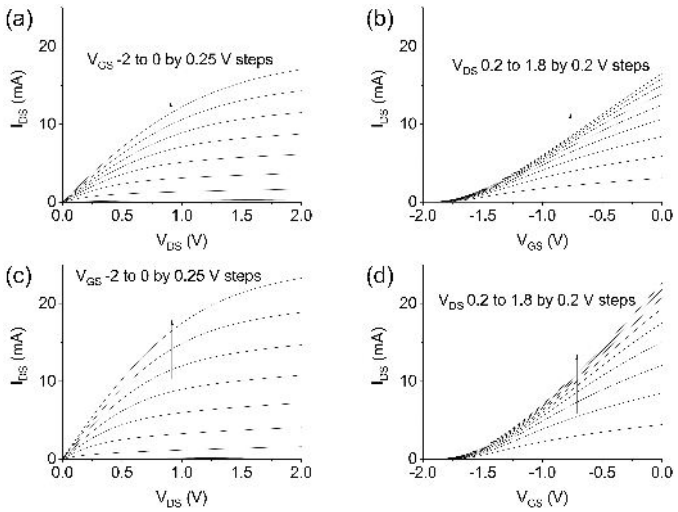

Fig. 2. (a) JFETJC I_{DS} versus V_{DS}. (b) JFETJC I_{DS} versus V_{GS}. (c) JFETLN I_{DS} versus V_{DS}. (d) JFETLN I_{DS} versus V_{GS}.

JFETJC exhibits more than ten times worse flicker noise than comparable MOSFET devices due to the presence of this STI. In our modified JFET device (JFETLN, Fig. 1b), breakdown voltages exceed 8 V, but flicker noise power is reduced by a factor of 100 when compared to the JFETJC. Our techniques are adaptable to many advanced CMOS technology nodes, allowing low-noise JFETs to be supported with few changes to a standard triple-well process.

II. Device Results

For the JFETLN device developed here, we replace the STI isolating the top gate implant with a polysilicon (PC) blocking layer, which also breaks the silicide between the n-channel and top gate, as shown in Fig. 1b. The polysilicon is electrically unused and is left floating, acting only to increase lateral isolation between top gate and channel diffusions. We also created geometric variants, including a waffle-style JFETLN, as shown in Figs. 1c and 1d. This JFET has a small drain, surrounded by gate and source. This allows for the design of well-matched layouts of multiple transistors with a shared source and individual drains. Fig. 1e shows interdigitated waffle JFETLN devices used as a differential pair.

Measured IV characteristics of the JFETJC and JFETLN are shown in Fig. 2. Device transconductance per unit width for the shortest achievable channel length (500 nm) is typically 20.1 mS/mm (16.8 mS/mm) for the JFETLN (JFETJC). This compares with 23.7 mS/mm for a 0.5-μm-long PFET and 44.2 mS/mm for a 0.5-μm-long NFET in this technology. The measured JFETJC and JFETLN input capacitances as a function of V_{GS} are shown in Fig. 3a. The 0.5-μm-long JFETLN has an input capacitance between 4.4 and 5.9 fF/μm^2 of gate area in the typical region of operation (V_{GS} between -2.0 and -1.0 V), while the JFETJC has between 4.4 and 5.4 fF/μm^2. In contrast, the measured NFET input capacitance for a 0.5-μm-long device, shown in Fig. 3b, ranges from 5.8 to 8.6 fF/μm^2 in the typical region of operation (V_{GS} between 0.5 and 1.0 V). The decrease in capacitance observed for the

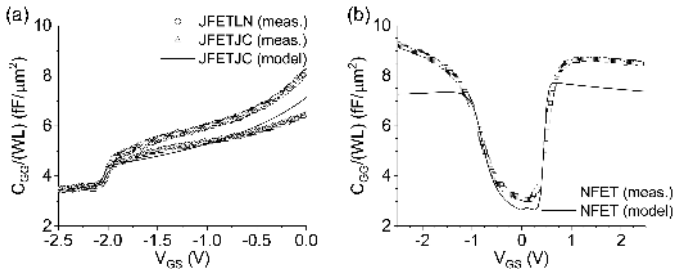

Fig. 3. (a) Measured JFETLN input capacitance per gate width compared to JFETJC measured and model capacitance. (b) Measured NFET input capacitance per gate width compared with the NFET model.

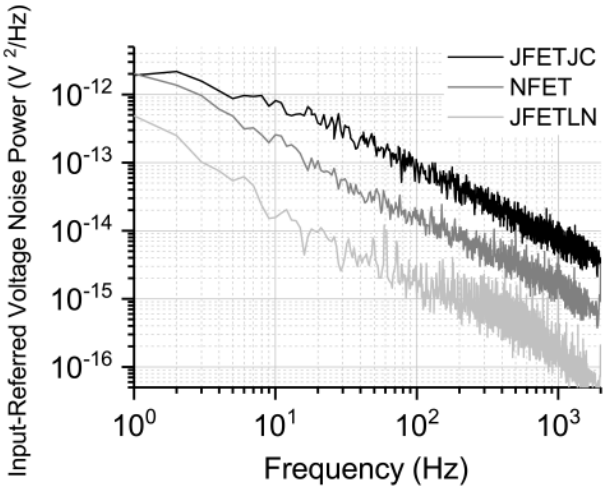

Fig. 4. Input-referred noise spectral density of JFETJC, JFETLN, and NFET devices.

JFETLN and JFETJC for V_{GS} less than -2 V is caused by the body becoming fully depleted, resulting in a reduction in the gate-to-channel capacitance [13]. The JFETLN has slightly higher input capacitance than the JFETJC for V_{GS} above -2 V due to an increase in the gate-to-source junction area caused by the removal of the STI, as seen in Figs. 1a and 1b.

The input flicker noise power of the JFETJC, NFET, and JFETLN are shown in Fig. 4 for devices with the same layout width (320 μm, as sixteen 20 μm fingers), length (500 nm), and current density (3.125 mA/mm). The input flicker noise power of the JFETLN is around a factor of 100 lower than the JFETJC. In comparison with the NFET noise spectrum, the JFETLN has more than ten times lower input-referred flicker noise power. We used NFETs in these comparisons because the JFETJC, JFETLN, and NFET all support similar circuit topologies. An equally sized PFET in this technology still has more than four times the input-referred flicker noise as the JFETLN. The thermal noise performance is well predicted by the device transconductance. In this technology, the JFET devices have lower transconductance than NFET devices and comparable transconductance to the PFET devices. Therefore, the thermal noise performance of the JFET and PFET are comparable and higher than that of the NFET. The corner frequency for the JFETLN devices is approximately 4 MHz.

We fit the 1/f noise using an empirical model of the form: $S_n(f) = SI_D{}^{\alpha} f^{\beta}$, where I_D is the drain current, S is the total

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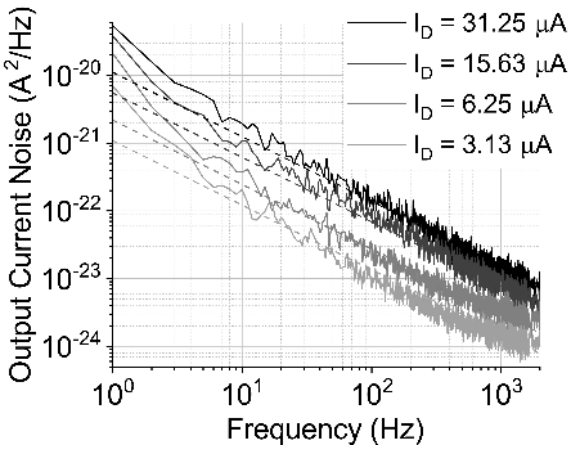

Fig. 5. JFETLN output-referred current noise and multi-linear model fit.

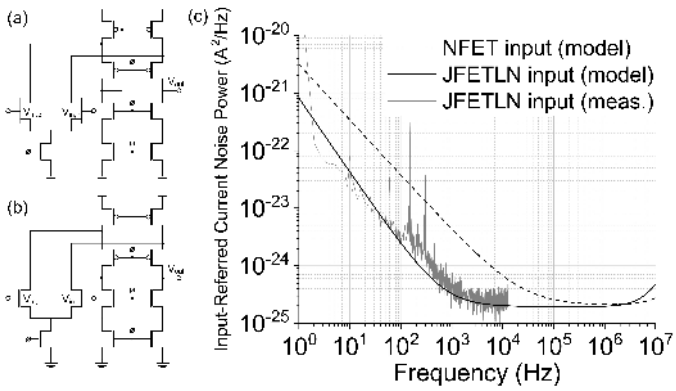

Fig. 6. (a) JFETLN-input OTA schematic. (b) NFET-input OTA schematic. (c) Input-referred current noise of JFETLN-input TIA compared with the simulation of JFETLN-input and NFET-input TIAs.

flicker noise coefficient, α is the current exponent, and β is the frequency exponent. The fit is then applied to noise curves at multiple current levels using a multilinear least-squares regression, as shown in Fig. 5, for a waffle-style JFETLN (W = 10 μm, L = 500 nm). This fit results in noise coefficients of: $S = 4 \times 10^{-16}$, $\alpha = 1.01$, and $\beta = -0.95$. These values are used in a Verilog-A compact model based on the JFETJC model, which is employed for circuit simulations.

III. Noise-optimized Amplifiers with JFET Inputs

Using this Verilog-A compact model developed for the JFETLN, we designed, built, and tested a low-noise JFETLN-input OTA seen in Fig. 6a. This design uses two waffle-style JFETLN devices as the input differential pair. For comparison, an NFET-input OTA design (Fig. 6b) was also simulated based on the same circuit design with the input transistors changed to NFETs. We preserved the geometry and bias currents across the two designs and set the DC bias configuration to keep both input pairs in saturation.

To verify the accuracy of the JFETLN model, we implemented the OTA in a transimpedance configuration. The JFETLN-input amplifier has superior input-referred noise performance for bandwidths up to 1 MHz when compared to the simulated NFET-input design, as shown in Fig. 6c. The noise is reduced by up to 10 times versus the simulated NFET design. We used a feedback resistor of 1 MΩ and measured a gain of 986.7 kΩ. The input current was supplied via a 100 kΩ resistor to ground, to limit added noise. The measured noise for the JFETLN TIA agrees well with the simulation. Near 1 MHz, the current noise from the feedback resistor begins to dominate for both OTAs. Also, the thermal noise caused by the lower transconductance of the JFETLN begins to overwhelm the gains from the lowered flicker noise. These low flicker noise JFET OTAs are useful for constructing integrated preamplifier stages in the 1 Hz – 1 MHz range, facilitating a variety of low-noise sensor applications.

IV. Conclusion

We created new low-noise CMOS-integrated JFET structures in a standard 0.18 μm CMOS process. These devices are ideal for low-noise transimpedance and voltage-mode amplifiers for bioelectronics applications due to flicker noise power that is a factor of 10 smaller than NFET transistors of the same size. Consequently, when utilized in place of NFET transistors for the input stage of transimpedance amplifiers at the same length, width, and current bias, the input-referred noise can be reduced by up to a factor of 10. These low-noise JFETs are well-suited for improving the performance of CMOS integrated amplifiers for bioelectronics applications due to their reduced flicker noise, reduced input capacitance, and CMOS-compatibility.

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