Integrated-Circuit Node for Time-Domain Near-infrared Diffuse Optical Tomography Imaging Arrays with On-chip Histogramming and Integrated VCSELs

Sajjad Moazeni*[1,2], Kevin Renehan*[1], Eric H. Pollmann[1], Kenneth L. Shepard[1]

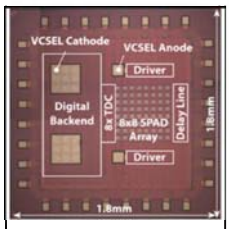
[1]Columbia University, New York, NY [2]University of Washington, Seattle, WA *Equal Contribution

Next-generation brain-computer interfaces (BCI) for healthy individuals largely rely on non-invasive functional imaging methods to record cortex-wide neural activity because of the risk associated with surgically implanted devices. Near-infrared (NIR) time-domain diffuse optical tomography (TD-DOT) is a promising non-invasive imaging approach which relies on reduced optical scattering and absorption of the human skull and brain tissue in the NIR spectrum [1]. In TD-DOT imaging, the time-of-flight (ToF) of scattered photons is measured, improving on continuous-wave approaches. This method has the potential to allow for direct sensing of intracellular neural activity and hemodynamics at higher spatial resolutions than electroencephalogram (EEG) and at higher temporal resolution than functional magnetic resonance imaging (fMRI), while supporting more compact and cost-effective form factors.

In this work, we demonstrate the design of such an integrated-circuit node that can be arrayed on a wearable patch to perform NIR TD-DOT with mm-range spatial resolution (Fig. 1). The node contains not only light emitters and detectors but also all the crucial electronics required to perform distributed TD-DOT imaging. Since achievable spatial resolution in TD-DOT is directly related to the node pitch, there is a need for a compact integrated element at each node which also facilitates scaling up to larger numbers of nodes as well.

During each recording frame, one or more of these nodes are configured to act as light sources to send a programmable number of short laser pulses into the tissue, while all nodes simultaneously perform ToF measurement of detected photons. The resulting arrival-time histograms provide information about both the scattering and absorption of the tissue in the optical path. Later arriving photons represent absorption in deeper regions-of-interest (ROIs) as shown in Fig. 1. For brain imaging, the majority of early-arriving photons are non-informative, since they are backscattered off of the skull [1, 2]. As a result, it is important for the nodes be able to gate these photons away to improve imaging contrast, increase the dynamic range of detection and to avoid pile-up distortion by rejecting these skull-backscattered photons which dominate in the case of sub-cm source-detector pitch configurations [2,3]. The presence of time-dependent absorption within a ROI (e. g., due to hemodynamics) modulates the properties of histogram tails. By measuring and collecting histograms at each site on the wearable patch, a time-dependent tomographic model can be constructed using inverse imaging algorithms based on radiative transfer equations (RTE) [1].

Each node consists of an integrated circuit chip containing an 8x8 single-photon avalanche diode (SPAD) array and two vertical cavity surface emitting lasers (VCSEL), to support dual-wavelength operation, stacked directly onto the chip surface on their cathode (bottom plate) while the anode signals are wire-bonded to the on-chip drivers. Fig. 2 shows the system-level block diagram of the node electronics. All the chips on a patch can be synchronized and triggered together through a shared external reference clock. The SPAD array has a dedicated event-driven time-to-digital converter (TDC) per row, which together can support detection and ToF measurement of up to eight photons simultaneously. SPADs are operated by in-pixel active quench and reset circuits (AQC) with tunable delays to control time-gating, optimized to operate at 100MHz repetition rate. TDCs are implemented using asynchronous control logic and a four-stage ring-oscillator employing pseudo-differential inverter cells with a cross-coupled PMOS load. Fig. 3 shows the circuit diagram of AQC and TDC inverter cells. The TDC outputs are generated by reading and decoding the oscillator's internal state (three fine bits) and the number of oscillation cycles (seven coarse bits) and are fed into subtractor blocks, where a programmable correction is introduced to remove the offset caused by the event-driven operation of the TDC as well as any other systematic and chip-to-chip timing variations. This facilitates a large reduction in the number of histogram bins, reducing required chip bandwidth to 12.5Mb/s. The outputs of all eight subtractors flow to a bank of accumulators, where the ToF measurements collected by the eight data-paths aggregate to a single histogram per chip with 150 12-bits bins. Finally, the histogram is serialized in the data transmitter (Tx) block and transmitted to a central FPGA unit at the end of each frame. The chip operates independently after initial configuration, with the number of laser pulses monitored with a 15-bit counter and histogram stream out triggered when the counter reaches a programmable value.



Die micrograph.

A micrograph of the 1.8x1.8mm^2 node chip, fabricated in a 130nm high-voltage CMOS process, is shown above. SPADs are implemented with an 11µm-diameter active area using a custom doping implant. Pixels have a 60µm pitch with 3% effective fill-factor (FF). SPADs achieve photon detection probabilities (PDPs) of 21.7% and 10.5% at 670nm and 850nm wavelengths, respectively, at a 1.5V excess-bias voltage with a median dark-count rate (DCR) of 6.9cps and 115.5ps FWHM jitter (Fig. 4). 670nm VCSELs (Vixar Inc.) are operated with tunable optical power of up to 3mW and pulse-width of ~300ps. TDCs have been characterized using an external pulse generator from the median of 50 samples. Measurements show ~70ps timing resolution (LSB) over the entire range of ~70ns, which allows the chip to support repetition-rates as low as 10MHz. TDCs' FWHM jitter is less than 0.45LSB with the median DNL and INL of 0.52LSB and 3LSB across the entire TDC range, respectively.

Initial device characterization and calibration have been performed by measuring the ToF using two nodes and a mirror at multiple heights (z) under low-photon intensity to avoid pile-up. Fig. 5 depicts the schematic of this test setup along with three sample histograms. The peak and FWHM of each histogram for the 1cm to 6cm z-range is plotted showing the expected linear relation with one LSB per every 2cm ToF (~67ps) and a 3-LSB FWHM. Performance summary and comparison with prior work is also presented in Fig. 6. Each TDC consumes 17.5uA dynamic power at 500kS/s with 3mA static current drawn by PMOS current-bleeders to boost oscillator's frequency and achieve the target LSB. Total power consumption is 80mW under ambient light condition with 32mW and 5mW consumed by the digital backend and the VCSEL driver at 100MHz clock rate, respectively.

The effectiveness of time-gating to improve the imaging contrast is evaluated by measuring the absorption coefficient changes in a brain-tissue phantom (a mixture of milk and India ink) through a 5mm-thick skull phantom (a mixture of TiO_2 and epoxy resin). Fig. 6 shows un-gated and gated histograms with ~0.8ns gating delay (gated histogram is adjusted to align with the time-gating window) for two various ink concentrations. The image contrast is derived from $(N_0\text{-}N)/N_0$ equation, where N_0 and N denote unperturbed (no ink) and perturbed (with ink) photon counts, respectively. These plots confirm that gating improves the contrast by more than 25% in this case.

The single-chip TD-DOT node with integrated light-sources presented here is an important building block for scalable, wearable NIR imaging arrays. Potential applications extend beyond brain imaging to applications such as breast cancer detection.

Acknowledgments:
We gratefully acknowledge TSMC for providing fabrication support for the SPADs employed here. This work was supported by DARPA under Contract N66001-19-C-4020.

References:

[1] G. Strangman et al., "Non-invasive neuroimaging using near-infrared light," Biol Psychiatry, Oct. 2002.
[2] A. Puszka et al. "Spatial resolution in depth for time-resolved diffuse optical tomography using short source-detector separations," Biomedical optics Express, Dec. 2014.
[3] A. Tosi et al., "Fast-gated single-photon counting technique widens dynamic range and speeds up acquisition time in time-resolved measurements," Optics Express, May 2011.
[4] J. M. Pavia et al., "A 1x400 Backside-Illuminated SPAD Sensor With 49.7ps Resolution, 30pJ/Sample TDCs Fabricated in 3D CMOS Technology for NIR Optical Tomography," JSSC, Oct. 2015.
[5] C. Veerappan et al., "A 160x128 single-photon image sensor with on-pixel 55ps 10b time-to-digital converter," ISSCC, Feb. 2011

2021 IEEE Custom Integrated Circuits Conference (CICC) | 978-1-7281-7581-2/20/$31.00 ©2021 IEEE | DOI: 10.1109/CICC51472.2021.9431526

978-1-7281-7581-2/21/$31.00 ©2021 IEEE

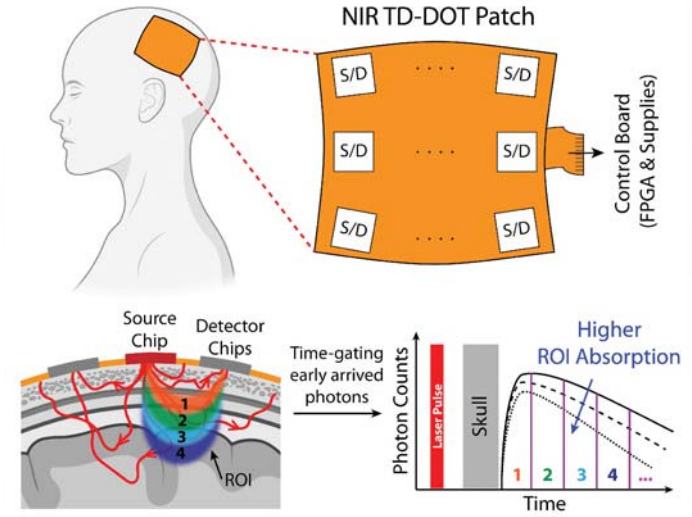


Fig. 1. NIR TD-DOT wearable device for non-invasive brain functional imaging using an array of proposed integrated-circuit nodes (S and D stand for source and detector, respectively).

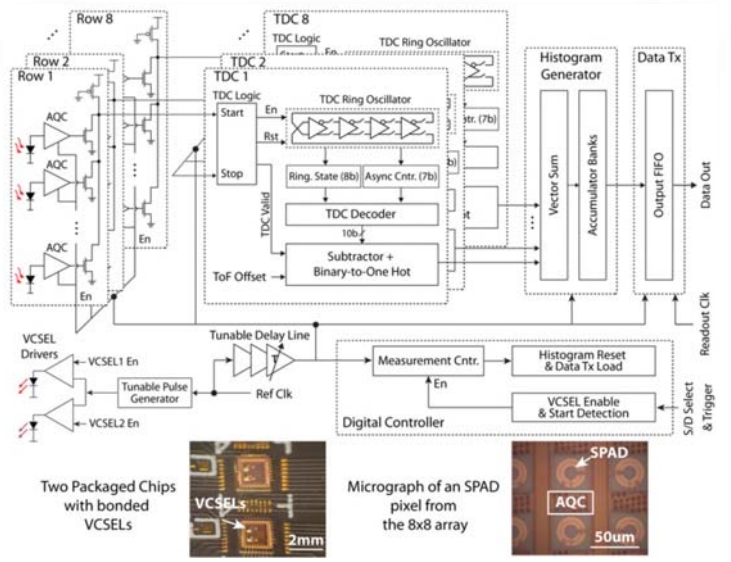


Fig. 2. Block-diagram of the CMOS integrated circuit node and micrographs of chips with bonded VCSELs and an SPAD pixel.

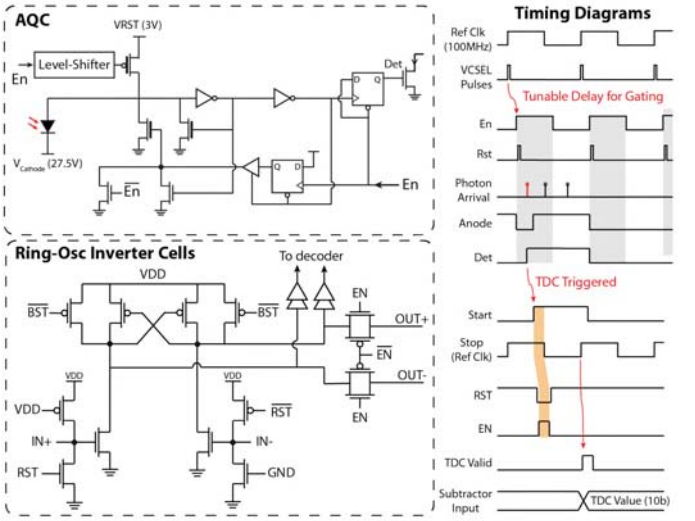


Fig. 3. Circuit diagrams of the AQC with optimized reset feedback-path's delay to operate at 100MHz, TDCs' inverter delay-cells, and timing diagrams of overall node operation.

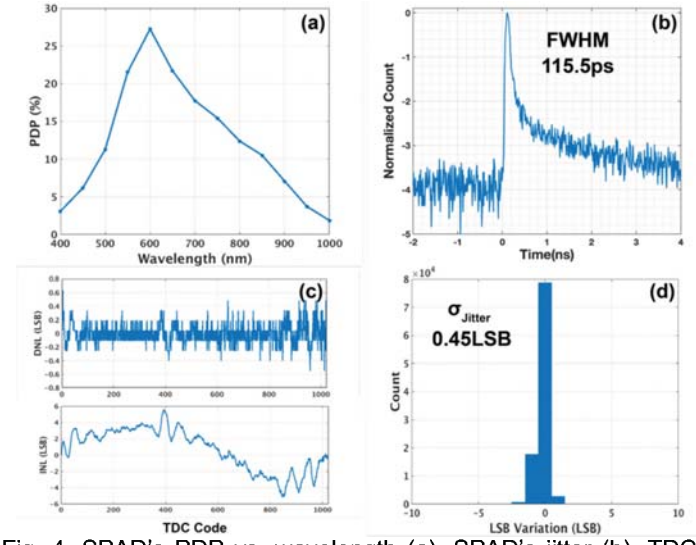
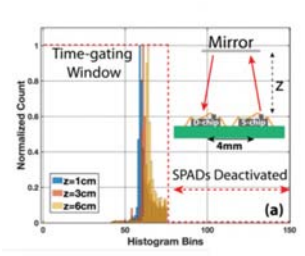
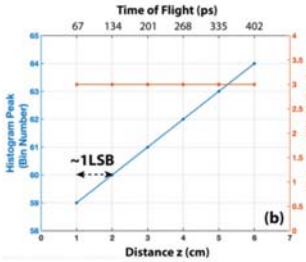


Fig. 4. SPAD's PDP vs. wavelength (a), SPAD's jitter (b), TDC's DNL and INL (c), and TDC's jitter measurement for a fixed delay of 10ns from a total of 100k measurements (d).





	Reference	JSSC' 15 [4]	ISSCC' 11 [5]	This Work
SPAD	Wavelength (nm)	800	637	670 / 850
	PDP (%)	12.2	19	21.7 / 10.5
	FF (%)	23.3	1	3
	DCR (Hz)	35k	50	6.9
	Jitter FWHM (ps)	260	140	115.5
TDC	Range (ns)	200	55	70
	DNL/INL (LSB)	0.44 / 0.47	0.3 / 2	0.52 / 3
	Resolution (ps)	49.7	55	70
	Jitter FWHM (LSB)	1.21	N/R	0.45
	Dynamic Power (uW) @500kS/s	15	N/R	17.5
System	Technology	CMOS (3D) 130nm	CMOS 130nm	CMOS 130nm
	Power (mW)	7*	550	80
	Array Size	1x400	160x128	8x8
	Chip area (mm²)	0.77x5	11x12.3	1.8x1.8
	Repetition Rate (MHz)	40	16	100
	Readout Data-rate (Gb/s)	1.040	51.2	0.0125
	Integrated Light Source	No	No	Yes

* Core only and under dark condition.

Fig. 5. ToF measurements: sample histograms for multiple chip-mirror distances (a) and histograms' peak and FWHM (b), and the summary of performance and comparison to prior works.

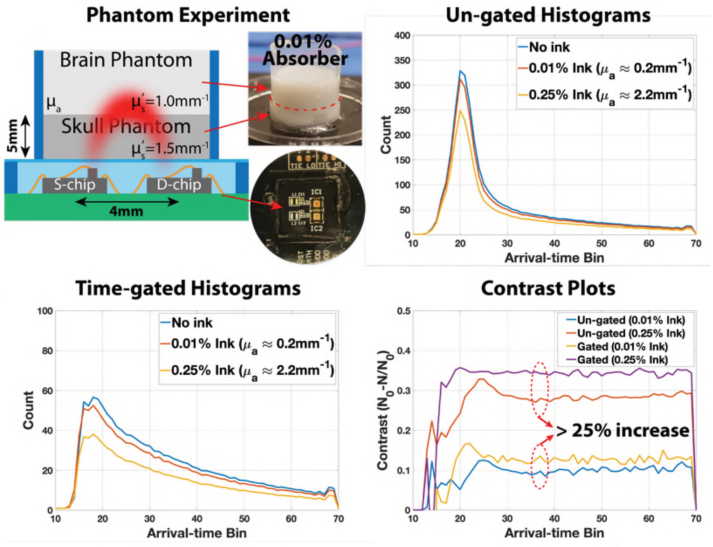


Fig. 6. NIR TD-DOT measurement using phantoms: experiment setup (μ_s': reduced scattering coefficient), arrival-time histograms with and without gating, and the imaging contrast comparison plots.