Fully Implantable 192×256 SPAD Sensor with Global-Shutter and Micro-LEDs for Bidirectional Subdural Optical Brain-Computer Interfaces

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Abstract— **We demonstrate a fully implantable optoelectronic neural interface device featuring an array of single-photon avalanche photodiode (SPAD) detectors with a global shutter and monolithically integrated with an array of flip-chip bonded micro-LEDs (μLED) for fluorescence excitation and optogenetic stimulation. The device is integrated with optical filters and a lens-less computation mask to create a 200-μm-thick implantable device. To enable the global shutter, an area-efficient 10b roll-over counter is used in-pixel. With a phase unwrapping algorithm, these counters can be used in a "modulo" fashion providing high dynamic range extension. Our SPAD sensor architecture achieves a better noise·power figure-of-merit (FoM) than comparable photodiode image sensors.**

Keywords—optoelectronic implants, single photon avalanche diodes, optogenetics, heterogeneous co-integration, brain computer interfaces.

I. INTRODUCTION

Neural interfaces play a significant role in exploring and understanding the brain. Despite the primacy of electrophysiological neural implants, optical neural interfaces have drawn recent interest because of the ability to introduce cell-type specificity into recording and actuation. Current optical interfaces rely primarily on microscopes, which despite work on miniaturization, are volumetrically inefficient [1], physically occupying more space than the volume they image, making them impractical as implanted devices. The key to reaching the limits of miniaturization, for both electrophysiological and optoelectronic implants, is heterogenous integration onto a CMOS integrated chip. In this work, we extend upon our previous implantable optoelectronic platform [2] by significantly improving upon the sensitivity, dynamic range, and power consumption of the SPAD image sensor.

II. SYSTEM DESIGN

This subdural implant design is shown in Fig. 1. The device consists of an array of 256×192 monolithic SPADs with a global shutter for low-light-intensity imaging and dual color (blue and red) flip-chip bonded μLEDs as light sources for fluorescence excitation and optogenetic stimulation, respectively. Implementing global-shutter integration, more than 41.6dB improvement in sensitivity can be achieved compared to rolling-shutter SPAD imagers [2]. Optical co-integration of the fluorescence sources, filters, and computational mask and thinning of the CMOS chip brings the total device thickness to
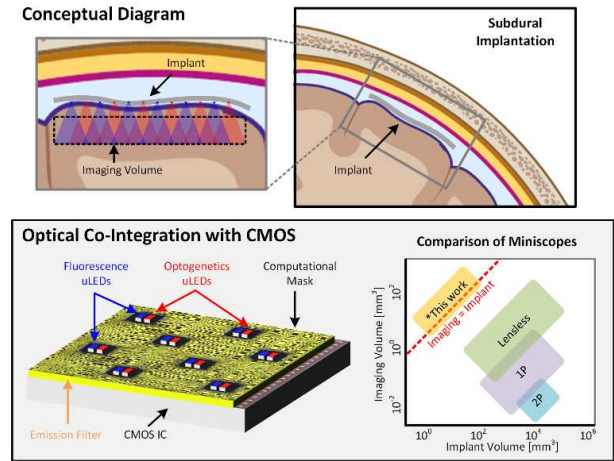

Fig. 1: Conceptual illustration of the fully-integrated neural implant.

less than 200 μm, making the implant volume of the imager less than the imaging volume of the tissue.

The imager controller is shown in Fig. 2. The chip's frame rate is 200fps, when reading the entire array, or 400fps, when reading half the array (128x192); the latter allows for the imaging of fast state-of-the-art voltage indicators [3]. The 100MHz RefClk supports the data transmission to meet the desired frame rate. The digital core operates on a divide by 8 DigClk to save power. Each pixel consists of two passively quenched SPADs whose outputs are combined into an in-pixel 10b counter. The data is read off the imager in a rolling column readout structure where the pixel data is buffered with up to 16 repeater cells throughout the array and loaded into a data serializer for streaming off chip. The *Col* signal allows for the data to reach the end of the array before the *Load* signal latches the data into the data serializer. Once the data is loaded, it is serialized off the chip at ~100Mbps.

The details of a single pixel are also shown in Fig. 2. The active diameter of each SPAD is 6μm; n-well sharing between the two adjacent chamfered square SPADs, as shown in the SPAD cross section, results in a fill-factor (FF) of 11.5%. The quenching circuit is passive-quench and passive-reset (PQRC) with dead-time determined by the VQ bias on the quench transistor. An off-pixel 3b digital to analog converter (DAC) provides the global VQ bias from 440mV to 1.06V in steps of 88mV. It uses the conventional resistor-divider topology for high linearity and consumes 800uW of power. To bring the
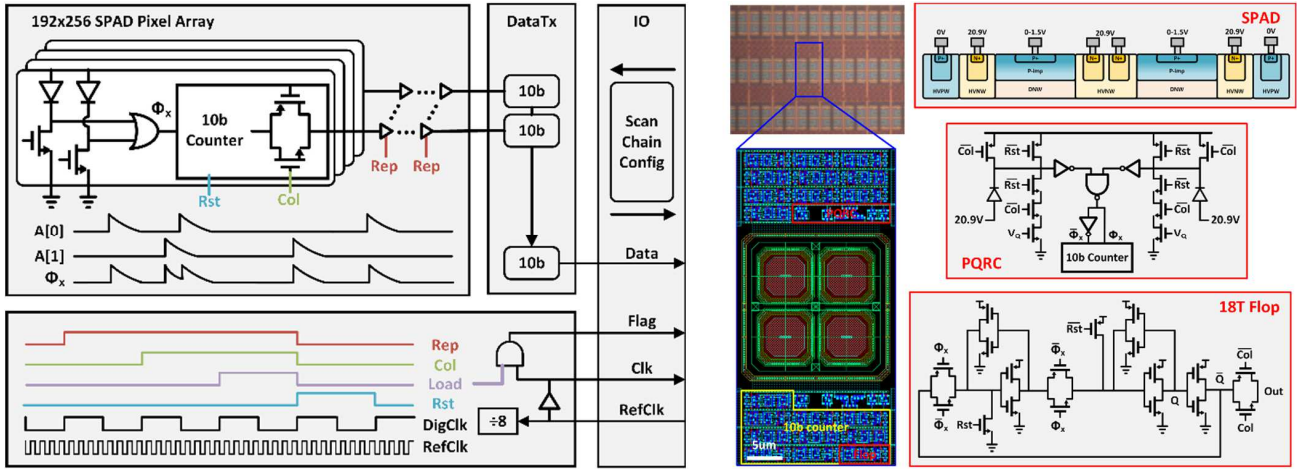
Fig. 2: Chip Block Diagram of SPAD pixel array, reset and readout waveforms, and data transmission. Schematic of SPAD, quenching circuit, and area-optimized flip-flop for 10b counter.

counter in-pixel, a divide-by-2 element was designed that uses an area-efficient custom 18T flip-flop circuit. The flip-flop is a positive-edge triggered, cross-coupled latch-based primary and replica design. The timing parameters of flip-flop support >2GHz photon arrival rate while consuming <3mW of power for the entire array at highest activity rate.

The µLED driver is designed to be compatible with various light emitting sources. The ANODE contact is global and be set above the turn-on voltage for a given light source. For example, blue OLEDs [4] and VCSELs [5] have relatively high turn ON voltages ~5-6V yet provide additional benefits such as high pixel density or narrow linewidth, respectively. The CATHODE contact has pixel-level control and can be modulated between ground and VDD.

III. SYSTEM VERIFICATION

The CMOS die shown in Fig. 3 is fabricated in a 0.13µm HV process. The SPADs are arrayed in blocks of 16×16 pixels with a pitch of 25µm. 12.5% of the array is removed for µLED bond pads and drivers. Commercially available, LA UB08FP2 (blue) and LA UR08FP2 (red) µLEDs, for fluorescence excitation and optogenetic stimulation, respectively, are flip chip bonded to the arrayed bond pads and are under filled with black epoxy (Epotek 320LV) to prevent light leakage. The spectrum of the blue µLED, conditioned by an interference excitation filter deposited
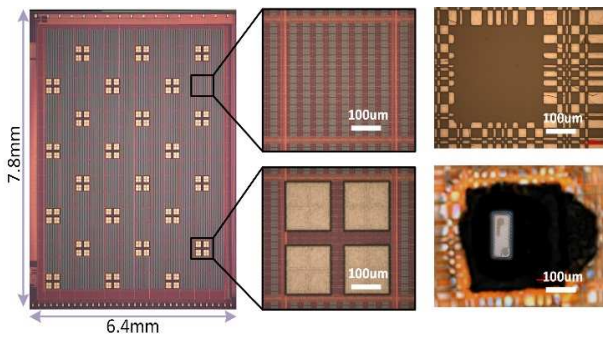
directly on the µLED surface, overlaps with commonly available fluorescence indicators.

The co-integration of the necessary optical components for fluorescence imaging as aware as the optical characterization are shown in Fig. 4. There are 24 blue and 24 red µLEDs arrayed across the imager and controlled via the scan chain. The measured IV-curves and optoelectronic efficiencies show the ideal operating point for each of the µLEDs. In addition to the excitation filter directly deposited onto the µLEDs, we co-
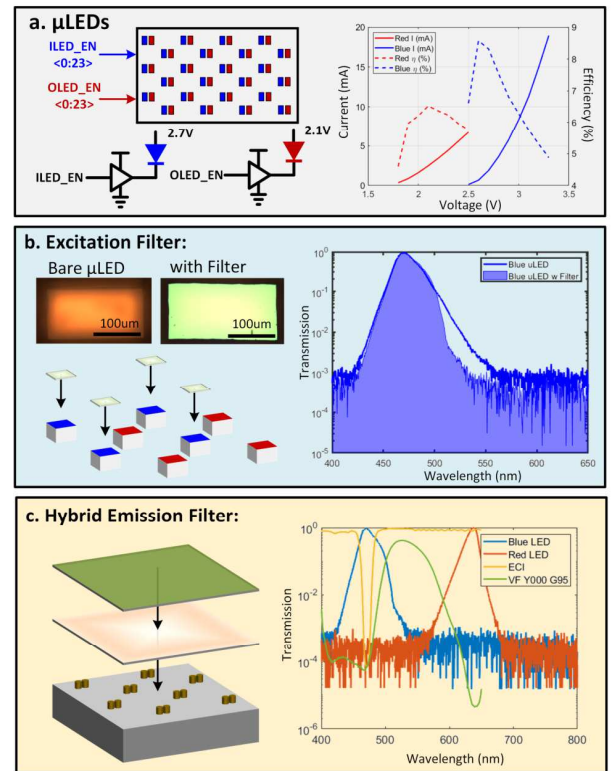

Fig 3. Die photo, SPAD array, and µLED pads fully packaged.

Fig. 4: a) Optical Characterization of µLEDs, b) Excitation Filter, and c) Hybrid Emission Filter.
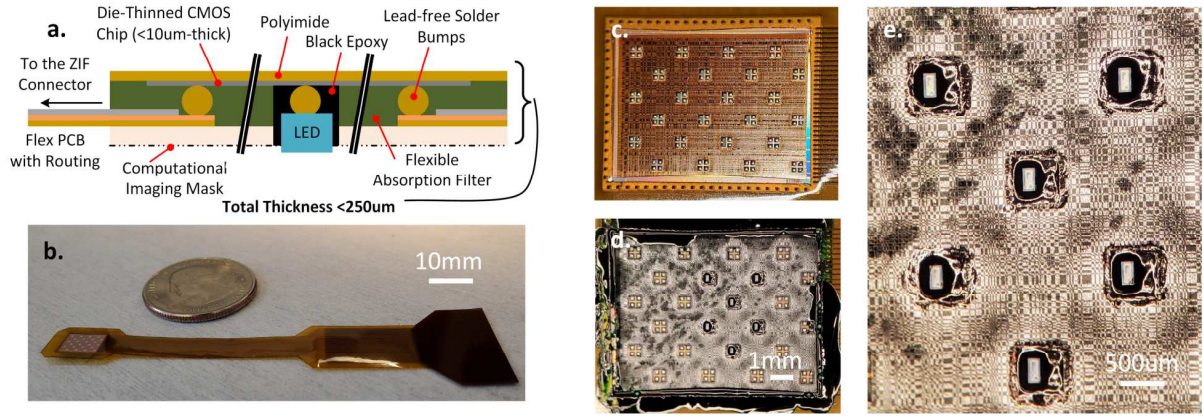
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Fig. 5: a) Cross-section of packaging stack up with <250µm thickness, b) Chip packaged with flexible PCB, c-d) Chip before and after epoxy underfill of the absorption filter, e) magnified image showing µLEDs and computational mask.

optimized a hybrid absorption/interference filter, which is deposited and packaged directly on the surface of the imager to reject the 470-nm blue excitation light in favor of 520-nm green emission with an optical density (OD) exceeding six.

The interference filter provides OD3 rejection over narrow spectrum and low angles of incidence (AOI), and the custom absorption filter provides additional OD3 rejection over a broader spectrum and all AOIs. The custom absorption filter is made by mixing Valifast Yellow 3150, Valifast Green 1501,

Fig. 6: a) SPAD photon detection probability and linearization with dynamic range extension, b) Computational mask calibration and double line slit reconstruction.

Cyclopentanone, and KMPR photoresist. The SPAD peak photon detection probability (PDP) is 9% at 550nm and the dark count rate is 17Hz at an excess bias voltage of 1.5V. Fig. 5 shows the final flexible packaging of the chip. The CMOS substrate is die-thinned as to become mechanically flexible and reduce its volumetric footprint for insertion underneath the dura.

The dynamic range of the image sensor determines the maximum and minimum signal intensities that can be recorded. Fluorescence signal is dependent on the absorption cross section and quantum efficiency of the fluorophore, the size and expression in the neuron, and the incident light flux. Any excitation light leakage or background fluorescence reduces the dynamic range. To enable the high-dynamic range required in fluorescence imaging, the chip operates as a modulo sensor [6], with counter wrapping at high intensity levels as shown in Fig. 6. The dynamic range of the sensor can be extended by a factor of 12 by this technique for an improvement from 60.2dB to 81.8dB. Furthermore, we leverage computational imaging techniques to obtain large field-of-view (FoV), high-resolution images without the use of focusing lenses. We employ the Texas Two-Step model for calibration and reconstruction of fluorescent point scenes [2, 7]. The double line slit reconstruction demonstrates a 50µm lateral resolution.

Finally, the inherent low-noise performance of SPADs, due to low dark-count rate (17Hz) and no read noise, enable low-power sensing which is important for implantable applications to limit tissue heating. Since the SPAD is an activity-based high-gain sensor, power consumption scales with light intensity, in contrast to photodiode imagers which rely on fixed amplification overhead. Our SPAD image sensor consumes ~18mW from VDD and ~160uW from the SPAD voltage in the dark. As the light intensity increases, the activity factor on VDD increases in the in-pixel counters and data transmission blocks. For medium light intensities, our chip consumes ~20mW from VDD and ~500uW from the SPAD voltage. Then, as the light levels increase and the counters start to rollover, VDD saturates around ~21mW and only the SPAD power consumption increases with light. Additionally, we measured the power draw from the cable drivers to be around 16mW. Future
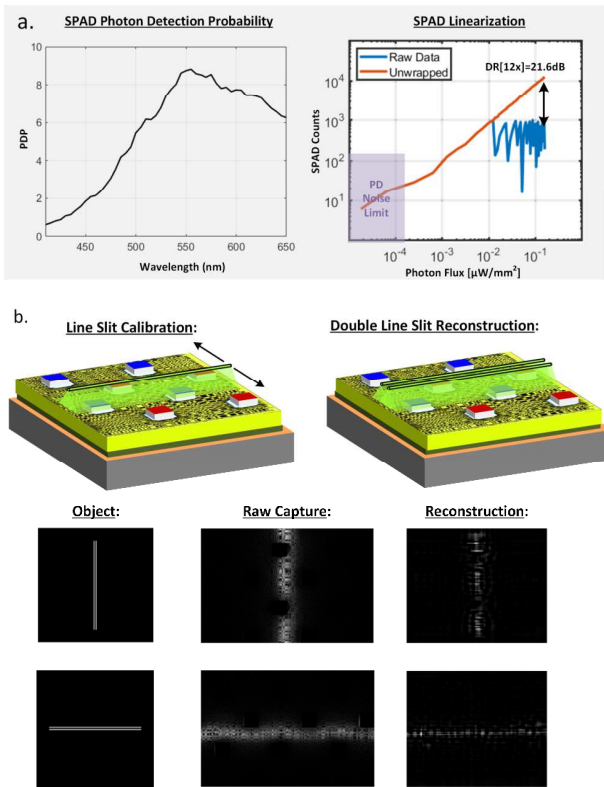
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SPAD Power

10b | IO

- Zero DC Power
- Light Dependent

20.9V

Low-Noise CIS Power

G → ADC → IO

- DC Power (G, ADC)
- Light Independent

3.3V

Total Chip vs SPAD Power

High Light Levels / Rollover

Medium Light Levels

SPAD Power scales with Light

VDD Power scales with activity factor

Dark Light Levels

SPAD vs CIS Figure of Merit [8]

- Single-Slope
- SAR
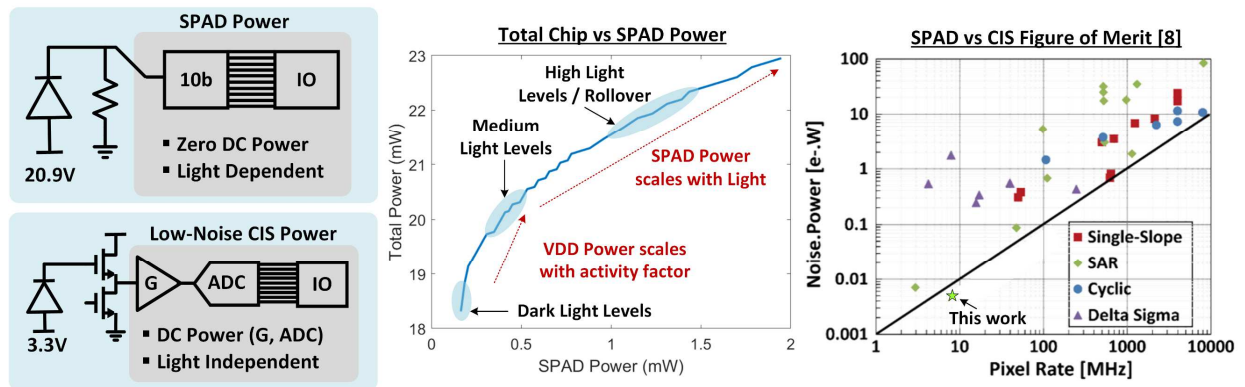- Cyclic
- Delta Sigma

This work

Fig. 7: Power consumption of the SPAD image sensor is light dependent while the low-noise CIS sensor has fixed overhead. VDD power scales with activity factor and saturates at medium light levels whereas SPAD power continues scaling with light. Comparison graph of CIS noise·power figure-of-merit [8].

implementations can use a more power-efficient data transmission module to further reduce power on VDD.

We compare our SPAD imager performance against a CIS noise-power figure-of-merit for low-light scenarios, commonly found in biological environments. The SPAD sensor pixel rate is defined as the number of pixels × the frame rate which is $192 \cdot 256 \cdot 200 fps$. The SPAD noise · power FoM is $\sqrt{DCR \times t_{int}} \cdot P \approx 0.087$ and it shows comparable or better FoM performance than low-noise CMOS image sensors [8] shown in Fig. 7. Comparison with current state-of-the-art [9, 10] is shown in Table 1.

	VLSI'14 [9]	VLSI'17 [10]	TBCaS'21 [2]	This Work
CMOS Technology	180nm	180nm	130nm	130nm
Pixel Pitch	35	55	30	25
FF/PDP (%)	14.4/2.7	28/5*(QE)	5/12	11.5/9
Dark Count (Hz)	200,000*	27fA	26	17
SPAD Array Size	72x60	80x36	160x160	256x192
Chief Ray Angle	10	18	70	70
Field of View (mm2)	2.1x2.5	4.7x2.25	5.4x5.4	5.1x6.8
Resolution	1000*	220	60	50
Frame-rate (fps)	N/R	20	125	200/400
Power (mW)**	83.8	3.5*	40	18 (VDD)
Data-rate (Mb/s)	N/R	N/A	40	100
Integrated Light Source	No	No	Yes	Yes

* Estimated from figures/data, ** Illumination power not included

Table 1. Comparison table with state-of-the-art.

IV. CONCLUSION

In this work, we improved upon the previous work with greater sensitivity, better spatial and temporal resolution, and larger pixel array. By achieving global shutter integration, we see a great improvement in sensitivity, allowing for low-power imaging of dim biological scenes. Future implementations can improve upon the resolution of the imager advanced technology nodes as well as utilize wireless power and data telemetry to achieve a truly implantable form factor.

ACKNOWLEDGMENT

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